NOVATEK

NT68F632

8-Bit Microcontroller for LCD Monitor (128K Flash Memory Type)

Section-1 General Description

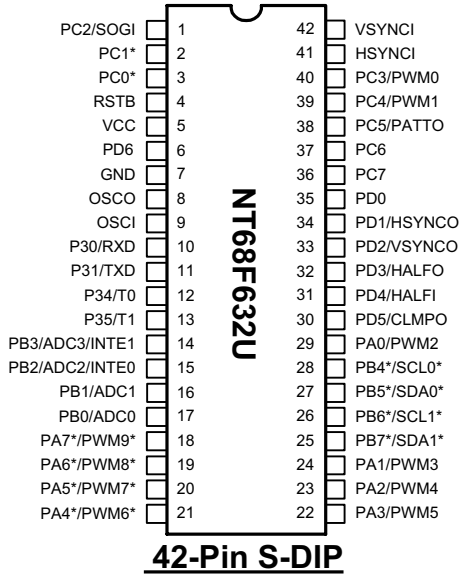
1-1 Features

- CMOS technology for low power consumption
- Operating voltage Vcc ranges from 3.0V to 3.6V
- 8031 8-bit CMOS Micro-Processor (uP) core
  - Intel compatible 8031 architecture
  - **256-byte** Internal DATA Memory
  - Two 16-Bit Timer/Counter
  - Fully duplex UART
  - 5-vector interrupt structure with two programmable priority levels
  - High level C-language for the F/W development
- On-Chip Oscillator ➨ 12MHz operating frequency
- 24MHz clock for CPU operating
- Reset
  - External Reset Pin
  - Low-Voltage Reset
  - Watch-Dog Timer Reset
  - ISP Reset
- Program memory
  - 128K bytes of on-chip flash memory for program memory
  - 2K bytes of Mask ROM for ISP control function
- 1,536 Bytes On-Chip RAM
  - Extended 256 Bytes Internal DATA Memory of uP 8031
  - External Data Memory
    - 768 Bytes General Purpose RAM Buffer（$F400 ~ $F6FF）
    - 512 Bytes RAM Buffer for hardware DDC Port（$F800 ~ $F9FF）
- A/D Converter
  - 7-Bit resolution
  - 4 selectable Input channels
  - Conversion Range ➨ Absolutely Monotonic linear from GND to VCC
  - Conversion time ➨ 12us
- PWM D/A Converter
  - 8-Bit resolution
  - 10 selectable output channels
    - 6 channels with 3.3V Push-Pull Structure
    - 4 channels with 5V Open-Drain Structure
- 35（37 for PLCC Package） Selectable General Purpose I/O Pins
- Interrupts ➨ 5-vector interrupt structure with two programmable priority levels for uP F8031
  - TF0: Timer/Counter 0 Overflow Interrupt
  - TF1: Timer/Counter 1 Overflow Interrupt
  - RI+TI: UART Interrupts
  - INT0:
    - Sync Processor Interrupts
    - I^2C Bus Port-0 (PB4, PB5) Interrupt
  - INT1
    - External Interrupts: INTE0 & INTE1
    - I^2C-Bus Port-1 (PB6, PB7) Interrupts
- Sync Processor Unit
  - Signal Type ➨ Separate Sync, Composite Sync & Digital-Level Sync-On-Green（SOG）
  - Powerful Polarity detection for HSYNCI and VSYNCI
  - HSYNCO/VSYNCO polarity-controlled outputs
  - Fast Auto-Mute function
  - Half frequency I/O function
  - Timer/Counters with 2-lay content latches for counting sync period/frequency ➨ stable results can be read
  - Clamp pulse output
    - Clamp pulse output at either the leading edge or trailing edge of HSYNC
    - Selectable Clamp pulse width
    - Selectable pulse output polarity
  - Flexible free-run H/V sync output generator
  - Flexible test pattern generator
- DDC Port
  - Dual indepentent input DDC channels
  - Pure hardware solution for VESA DDC1/2B
  - Selectable 128/256 Bytes EDID-Buffer for hardware DDC port
- I^2C-bus
  - Two built-in master/slave I^2C bus interfaces support VESA 2Bi/2B+
  - SCL clock speed supports up to 400Kbps
- Package
  - 42-Pin S-DIP
  - 44-Pin PLCC

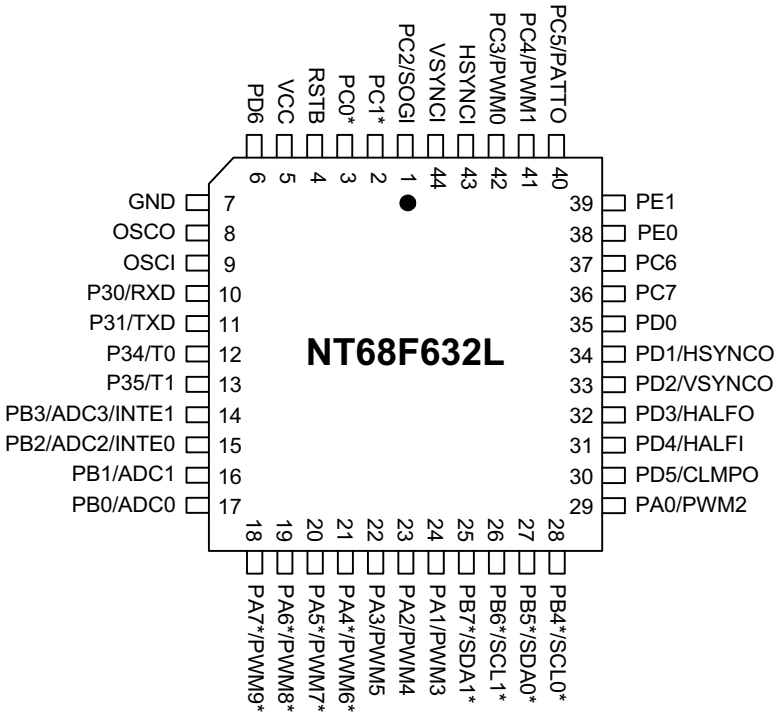
1-2 General Description

This is an 8031 CPU core embedded micro-controller, which is designed for the high-performance low-cost LCD monitor control application. It contains an 8-bit 8031 micro-controller, on-chip 128K bytes flash-type program ROM, 1,536-bytes internal data memory, four 7-bit resolution A/D Converter, 10-channel 8-bit resolution PWM DAC, two16-bit timer/counters, and an UART. Besides those, it has an internal SYNC processor, two-channel hardware DDC solution, and VESA 2Bi/2B+ master/slave I^2C bus interface. Those functions can help the user to develop a LCD monitor application as soon as possible.

1-3 Pin Configurations



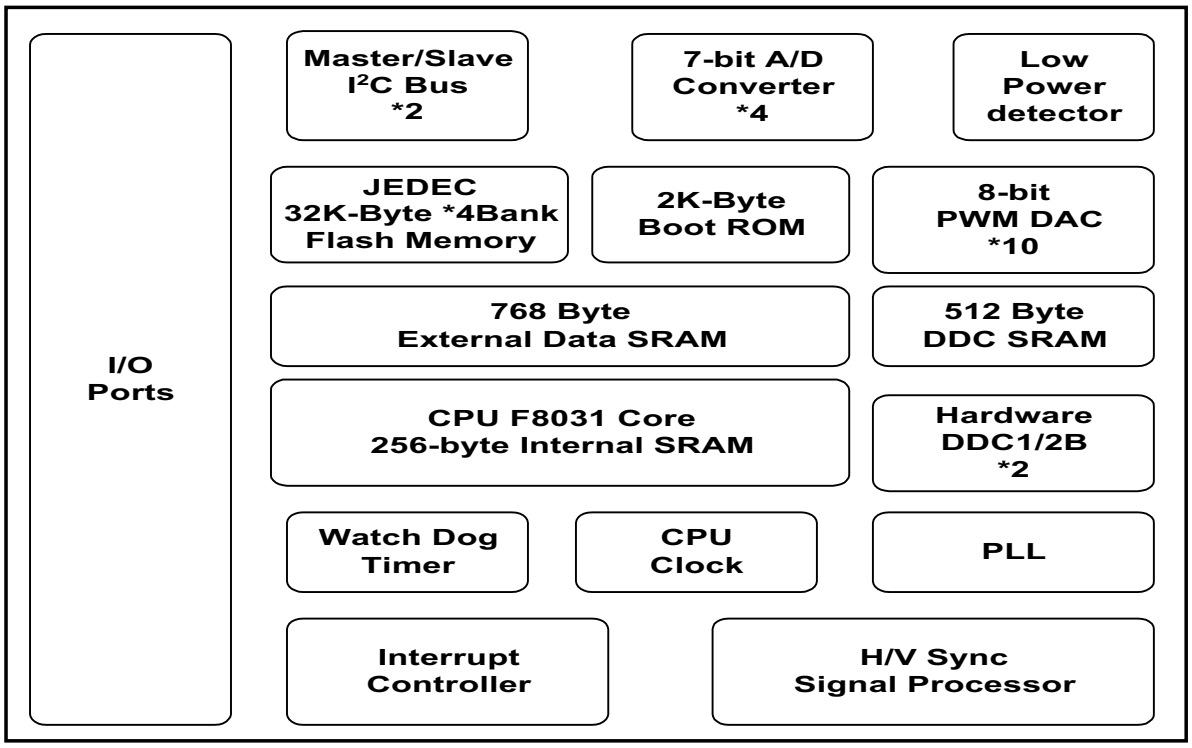
42-Pin S-DIP



44-Pin PLCC

Note: The "*" represents the *5V open-drain* structures.

1-4 Block Diagram



1-5 Pin Descriptions

Pin No.		Designation	Function	I/O	Description
44-Pin	42-Pin				
1	1	PC2/SOGI	**PC2**	**I/O**	**I/O Pin; Push-Pull Structure with Schmitt Trigger Input**
			SOGI	I	Digital-Level Sync-On-Green Sync Input; with Schmitt Trigger Input
2	2	PC1*	PC1*	I/O	I/O Pin; 5V Open-Drain Structure with Schmitt Trigger Input
3	3	PC0*	PC0*	I/O	I/O Pin; 5V Open-Drain Structure with Schmitt Trigger Input
4	4	RSTB	RSTB	I	Active-Low Reset Input; with Schmitt Triger Input
5	5	VCC	VCC	PWR	+3.3V Power Supply Input
6	6	PD6	PD6	I/O	I/O Pin; Push-Pull Structure with Schmitt Trigger Input
7	7	GND	GND	PWR	Power Ground
8	8	OSCO	OSCO	O	12MHz External Crystal OSC Output
9	9	OSCI	OSCI	I	12MHz External Crystal OSC Input
10	10	P30/RXD	**P30**	**I/O**	**GPIO Port-30 of Micro-Processor F8031**
			RXD	I	UART RX Data Input of Micro-Processor F8031
11	11	P31/TXD	**P31**	**I/O**	**GPIO Port-31 of Micro-Processor F8031**
			TXD	O	UART TX Data Output of Micro-Processor F8031
12	12	P34/T0	**P34**	**I/O**	**GPIO Port-34 of Micro-Processor F8031**
			T0	I	Counter/Timer T0 Input of Micro-Processor F8031
13	13	P35/T1	**P35**	**I/O**	**GPIO Port-35 of Micro-Processor F8031**
			T1	I	Counter/Timer T1 Input of Micro-Processor F8031
14	14	PB3/ADC3/INTE1	**PB3**	**I/O**	**I/O Pin; Push-Pull Structure with Schmitt Trigger Input**
			ADC3	I	A/D Converter Input-3; Hi-Z input
			INTE1	I	External Interrupt input 1; Schmitt Trigger Input
15	15	PB2/ADC2/INTE0	**PB2**	**I/O**	**I/O Pin; Push-Pull Structure with Schmitt Trigger Input**
			ADC2	I	A/D Converter Input-2; Hi-Z input
			INTE0	I	External Interrupt input 0, Schmitt Trigger Input
16	16	PB1/ADC1	**PB1**	**I/O**	**I/O Pin; Push-Pull Structure with Schmitt Trigger Input**
			ADC1	I	A/D Converter Input-1; Hi-Z input
17	17	PB0/ADC0	**PB0**	**I/O**	**I/O Pin; Push-Pull Structure with Schmitt Trigger Input**
			ADC0	I	A/D Converter Input-0; Hi-Z input

Pin Descriptions （Continued）

Pin No.		Designation	Function	I/O	Description
44-Pin	42-Pin				
18	18	PA7*/PWM9*	**PA7***	**I/O**	**I/O Pin; 5V Open-Drain Structure with Schmitt Trigger Input**
			PWM9*	O	PWM-Type D/A Converter; 5V Open-Drain Structure
19	19	PA6*/PWM8*	**PA6***	**I/O**	**I/O Pin; 5V Open-Drain Structure with Schmitt Trigger Input**
			PWM8*	O	PWM-Type D/A Converter; 5V Open-Drain Structure
20	20	PA5*/PWM7*	**PA5***	**I/O**	**I/O Pin; 5V Open-Drain Structure with Schmitt Trigger Input**
			PWM7*	O	PWM-Type D/A Converter; 5V Open-Drain Structure
21	21	PA4*/PWM6*	**PA4***	**I/O**	**I/O Pin; 5V Open-Drain Structure with Schmitt Trigger Input**
			PWM6*	O	PWM-Type D/A Converter; 5V Open-Drain Structure
22	22	PA3/PWM5	**PA3**	**I/O**	**I/O Pin; Schmitt Trigger Input**
			PWM5	O	PWM-Type D/A Converter; 3.3V Push-Pull Structure
23	23	PA2/PWM4	**PA2**	**I/O**	**I/O Pin; Schmitt Trigger Input**
			PWM4	O	PWM-Type D/A Converter; 3.3V Push-Pull Structure
24	24	PA1/PWM3	**PA1**	**I/O**	**I/O Pin; Schmitt Trigger Input**
			PWM3	O	PWM-Type D/A Converter; 3.3V Push-Pull Structure
25	25	PB7*/SDA1*	**PB7***	**I/O**	**I/O Pin; Open-Drain with Schmitt Trigger Input**
			SDA1*	I/O	5V Open-Drain Serial Data I/O Pin for the DDC Port 1 and the slave/master I^2C-Bus Port 1
26	26	PB6*/SCL1*	**PB6***	**I/O**	**5V I/O Pin; Open-Drain with Schmitt Trigger Input**
			SCL1*	I/O	5V Open-Drain Serial Clock I/O Pin for the DDC Port 1 and the slave/master I^2C-Bus Port 1
27	27	PB5*/SDA0*	**PB5***	**I/O**	**5V I/O Pin; Open-Drain with Schmitt Trigger Input**
			SDA0*	I/O	5V Open-Drain Serial Data I/O Pin for the DDC Port 0 and the slave/master I^2C-Bus Port 0
28	28	PB4*/SCL0*	**PB4***	**I/O**	**5V I/O Pin; Open-Drain with Schmitt Trigger Input**
			SCL0*	I/O	5V Open-Drain Serial Clock I/O Pin for the DDC Port 0 and the slave/master I^2C-Bus Port 0
29	29	PA0/PWM2	**PA0**	**I/O**	**I/O Pin; Schmitt Trigger Input**
			PWM2	O	PWM-Type D/A Converter; 3.3V Push-Pull Structure
30	30	PD5/CLMPO	**PD5**	**I/O**	**I/O Pin; Push-Pull Structure with Schmitt Trigger Input**
			CLMPO	O	Clamp Pulse Output for DC restoration of the Video Signal; Push-Pull Structure

Pin Descriptions （Continued）

Pin No.		Designation	Function	I/O	Description
44-Pin	42-Pin				
31	31	PD4/HALFI	**PD4**	**I/O**	**I/O Pin; Push-Pull Structure with Schmitt Trigger Input**
			HALFI	I	Half Frequency Input; Schmitt Trigger Input
32	32	PD3/HALFO	**PD3**	**I/O**	**I/O Pin; Push-Pull Structure with Schmitt Trigger Input**
			HALFO	O	Half Frequency Output; Push-Pull Structure
33	33	PD2/VSYNCO	**PD2**	**I/O**	**I/O Pin; Push-Pull Structure with Schmitt Trigger Input**
			VSYNCO	O	Vertical Sync Output; Push-Pull Structure
34	34	PD1/HSYNCO	**PD1**	**I/O**	**I/O Pin; Push-Pull Structure with Schmitt Trigger Input**
			HSYNCO	O	Horizontal Sync Output; Push-Pull Structure
35	35	PD0	PD0	I/O	I/O Pin; Push-Pull Structure with Schmitt Trigger Input
36	36	PC7	PC7	I/O	I/O Pin; Push-Pull Structure with Schmitt Trigger Input
37	37	PC6	PC6	I/O	I/O Pin; Push-Pull Structure with Schmitt Trigger Input
38	38	PC5/PATTO	**PC5**	**I/O**	**I/O Pin; Push-Pull Structure with Schmitt Trigger Input**
			PATTO	O	Test Pattern Output; Push-Pull Structure
39	39	PC4/PWM1	**PC4**	**I/O**	**I/O Pin; Push-Pull Structure with Schmitt Trigger Input**
			PWM1	O	PWM-Type D/A Converter; Push-Pull Structure
40	40	PC3/PWM0	**PC3**	**I/O**	**I/O Pin; Push-Pull Structure with Schmitt Trigger Input**
			PWM0	O	PWM-Type D/A Converter; Push-Pull Structure
41	-	PE0	PE0	I/O	I/O Pin; Push-Pull Structure with Schmitt Trigger Input **Only available in 44-Pin PLCC**
42	-	PE1	PE1	I/O	I/O Pin; Push-Pull Structure with Schmitt Trigger Input **Only available in 44-Pin PLCC**
43	41	HSYNCI	HSYNCI	I	Horizontal and Composite sync Input; Schmitt Trigger Input
44	42	VSYNCI	VSYNCI	I	VSYNC/Interrupt Input; Schmitt Trigger Input

Note: The " * " represents the open-drain structures.

Section-2 Memory Allocation

The standard uP F8031 can support up to 64K-byte external Program Memory size and 64K-byte external DATA Memory size. Now we expand the program memory up to 128K bytes by using the bank switching technique. And we have external 1,536 bytes of data memory for software develpoment. They are described as follows:

2-1 Program Memory

- 128K Bytes on-chip flash memory for user code.
- 2K Bytes mask-type Boot ROM for ISP function.

2-2 Data Memory

– Internal RAM：There are totally **256 bytes** internal DATA Memory of the uP F8031.

– Internal Special Function Registers (SFR)：There are **128 bytes** SFR, which is the internal reserved memory for system registers of the uP F8031.

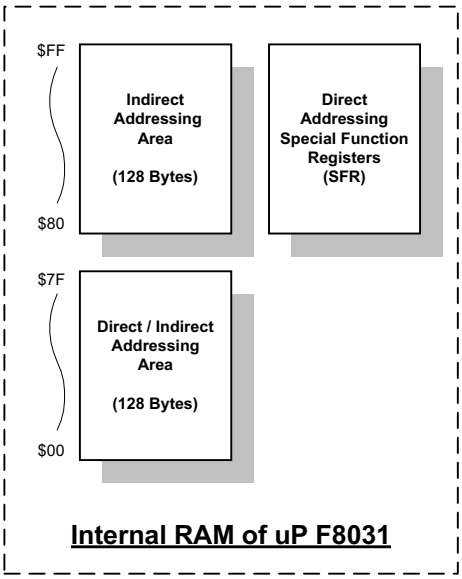
– External DATA Memory
  - **768** Bytes general purpose RAM buffer, address maping from $F400H to $F6FFH.
  - **512** Bytes external data memory reserved for EDID buffer of the Hardware DDC Port, range from $F800H to $F9FFH

2-3 Interrupt Vectors

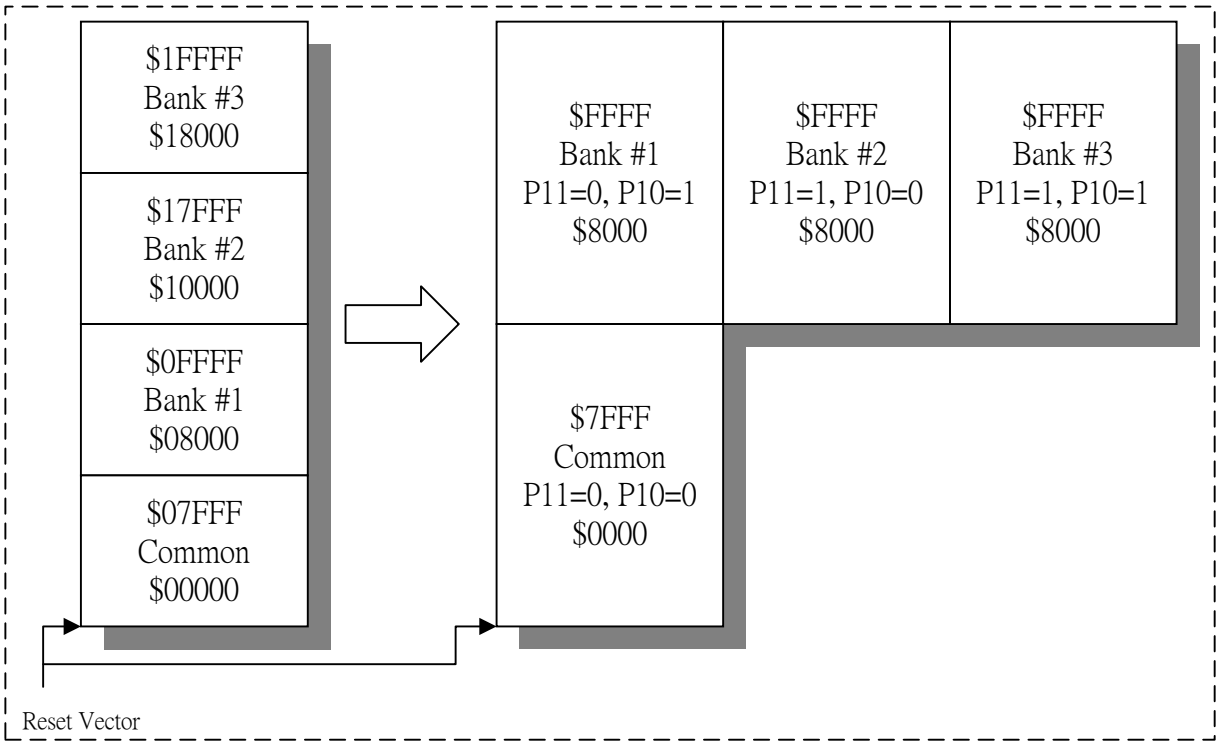
Address	Interrupt Source	Description
0000H	Reset	System Reset
0003H	IE0	External INT0 Interrupt of the uP F8031
000BH	TF0	Timer/Cunter 0 Overflow Interrupt of the uP F8031
0013H	IE1	External INT1 Interrupt the of uP F8031
001BH	TF1	Timer/Cunter 1 Overflow Interrupt of the uP F8031
0023H	RI & TI	UART Transmit interrupt & Receive interrupt of the uP F8031

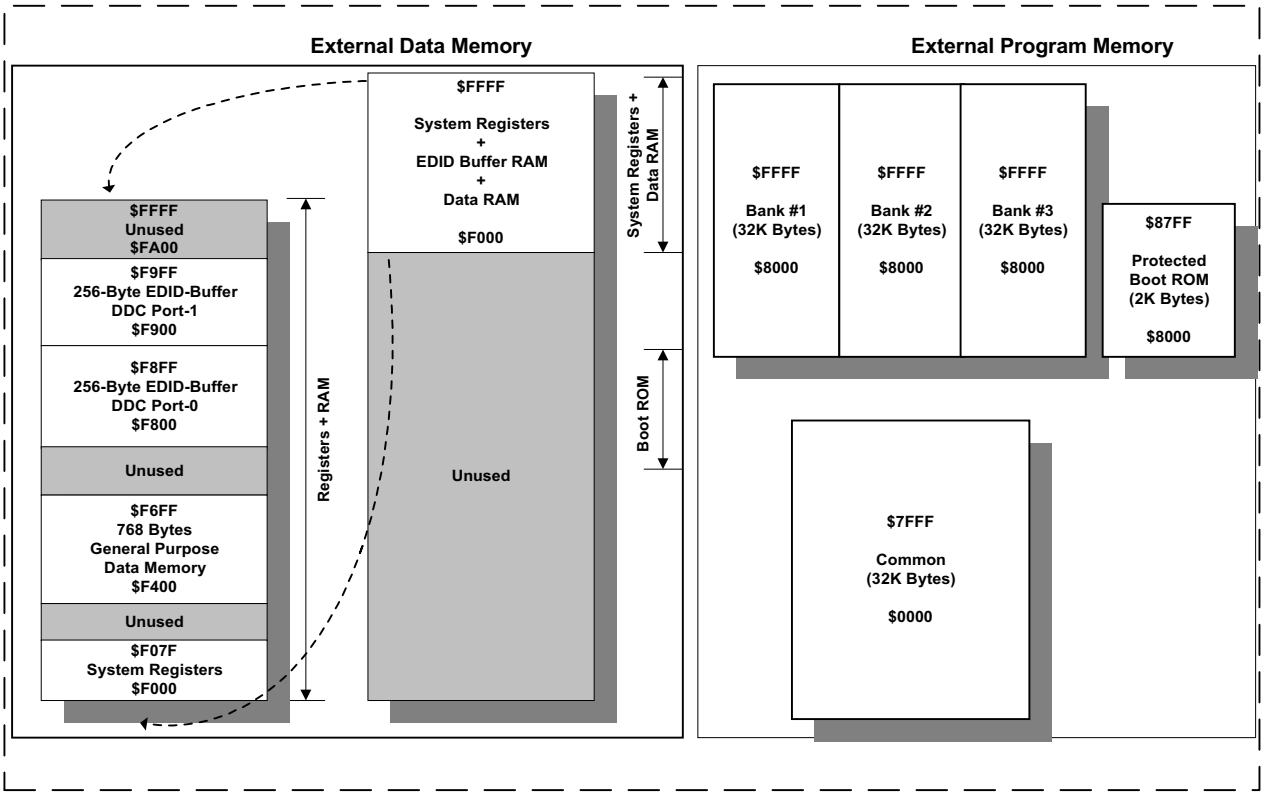
2-4 Memory Map

- The Internal Data Memory Map of the uP F8031 is configured as shown as below



- The External Memory Map in Normal Mode





External Memory Map of the uP F8031 in Normal Mode

2-5 System Registers

General I/O Ports Control Registers											
Addr.	**Name**	**Init.**	**R/W**	**Bit7**	**Bit6**	**Bit5**	**Bit4**	**Bit3**	**Bit2**	**Bit1**	**Bit0**
$F000	PortA	$0FH	R/W	PA7	PA6	PA5	PA4	PA3	PA2	PA1	PA0
$F001	PortB	$FFH	R/W	PB7	PB6	PB5	PB4	PB3	PB2	PB1	PB0
$F002	PortC	$FCH	R/W	PC7	PC6	PC5	PC4	PC3	PC2	PC1	PC0
$F003	PortD	$7FH	R/W	-	PD6	PD5	PD4	PD3	PD2	PD1	PD0
$F004	PortE	$03H	R/W	-	-	-	-	-	-	PE1	PE0
General I/O Ports R/W Direction Control Registers											
Addr.	**Name**	**Init.**	**R/W**	**Bit7**	**Bit6**	**Bit5**	**Bit4**	**Bit3**	**Bit2**	**Bit1**	**Bit0**
$F005	RDPA_REG	$0FH	R/W	RDPA_7	RDPA_6	RDPA_5	RDPA_4	RDPA_3	RDPA_2	RDPA_1	RDPA_0
$F006	RDPB_REG	$FFH	R/W	RDPB_7	RDPB_6	RDPB_5	RDPB_4	RDPB_3	RDPB_2	RDPB_1	RDPB_0
$F007	RDPC_REG	$FCH	R/W	RDPC_7	RDPC_6	RDPC_5	RDPC_4	RDPC_3	RDPC_2	RDPC_1	RDPC_0
$F008	RDPD_REG	$7FH	R/W	-	RDPD_6	RDPD_5	RDPD_4	RDPD_3	RDPD_2	RDPD_1	RDPD_0
$F009	RDPE_REG	$03H	R/W	-	-	-	-	-	-	RDPE_1	RDPE_0
Watch-Dog Timer Control Register											
Addr.	**Name**	**Init.**	**R/W**	**Bit7**	**Bit6**	**Bit5**	**Bit4**	**Bit3**	**Bit2**	**Bit1**	**Bit0**
$F00A	CLRWDT	$55H	W	0	1	0	1	0	1	0	1
A/D Converter Control Registers											
Addr.	**Name**	**Init.**	**R/W**	**Bit7**	**Bit6**	**Bit5**	**Bit4**	**Bit3**	**Bit2**	**Bit1**	**Bit0**
$F00B	ADC_CON	$00H	W	STRT_ADC	-	-	-	EN_ADC3	EN_ADC2	EN_ADC1	EN_ADC0
			R	-	-	-	-	EN_ADC3	EN_ADC2	EN_ADC1	EN_ADC0
$F00C	ADC0	$00H	R	-	AD06	AD05	AD04	AD03	AD02	AD01	AD00
$F00D	ADC1	$00H	R	-	AD16	AD15	AD14	AD13	AD12	AD11	AD10
$F00E	ADC2	$00H	R	-	AD26	AD25	AD24	AD23	AD22	AD21	AD20
$F00F	ADC3	$00H	R	CMP_ADC	AD36	AD35	AD34	AD33	AD32	AD31	AD30
PWM Channel Enable Control Registers											
Addr.	**Name**	**Init.**	**R/W**	**Bit7**	**Bit6**	**Bit5**	**Bit4**	**Bit3**	**Bit2**	**Bit1**	**Bit0**
$F010	ENPWM_LB	$00H	R/W	-	-	-	-	-	-	EN_PWM1	EN_PWM0
$F011	ENPWM_HB	$00H	R/W	EN_PWM9	EN_PWM8	EN_PWM7	EN_PWM6	EN_PWM5	EN_PWM4	EN_PWM3	EN_PWM2
PWM Channel 0~9 Control Registers											
Addr.	**Name**	**Init.**	**R/W**	**Bit7**	**Bit6**	**Bit5**	**Bit4**	**Bit3**	**Bit2**	**Bit1**	**Bit0**
$F012	PWM0	$80H	R/W	PWM07	PWM06	PWM05	PWM04	PWM03	PWM02	PWM01	PWM00
$F013	PWM1	$80H	R/W	PWM17	PWM16	PWM15	PWM14	PWM13	PWM12	PWM11	PWM10
$F014	PWM2	$80H	R/W	PWM27	PWM26	PWM25	PWM24	PWM23	PWM22	PWM21	PWM20
$F015	PWM3	$80H	R/W	PWM37	PWM36	PWM35	PWM34	PWM33	PWM32	PWM31	PWM30
$F016	PWM4	$80H	R/W	PWM47	PWM46	PWM45	PWM44	PWM43	PWM42	PWM41	PWM40
$F017	PWM5	$80H	R/W	PWM57	PWM56	PWM55	PWM54	PWM53	PWM52	PWM51	PWM50
$F018	PWM6	$80H	R/W	PWM67	PWM66	PWM65	PWM64	PWM63	PWM62	PWM61	PWM60
$F019	PWM7	$80H	R/W	PWM77	PWM76	PWM75	PWM74	PWM73	PWM72	PWM71	PWM70
$F01A	PWM8	$80H	R/W	PWM87	PWM86	PWM85	PWM84	PWM83	PWM82	PWM81	PWM80
$F01B	PWM9	$80H	R/W	PWM97	PWM96	PWM95	PWM94	PWM93	PWM92	PWM91	PWM90

System Registers （Continued）

Hardware DDC Port-0 Control Registers (PB4,PB5)											
Addr.	**Name**	**Init.**	**R/W**	**Bit7**	**Bit6**	**Bit5**	**Bit4**	**Bit3**	**Bit2**	**Bit1**	**Bit0**
$F01C	DDC_CTL0	$48H	R	EN_DDC	WPT_DDC	LEN_EDID	MODE	EN_BACK	INTV_CLK	-	UPD_DDC
		-	W	EN_DDC	WPT_DDC	LEN_EDID	MODE	EN_BACK	INTV_CLK	CLR_PTR	CLR_UPD
$F01D	DDC_ADDR0	$00H	W	VALID_3	VALID_2	VALID_1	-	ADDR_3	ADDR_2	ADDR_1	-
Hardware DDC Port-1 Control Registers (PB6,PB7)											
Addr.	**Name**	**Init.**	**R/W**	**Bit7**	**Bit6**	**Bit5**	**Bit4**	**Bit3**	**Bit2**	**Bit1**	**Bit0**
$F01E	DDC_CTL1	$48H	R	EN_DDC	WPT_DDC	LEN_EDID	MODE	EN_BACK	INTV_CLK	-	UPD_DDC
		-	W	EN_DDC	WPT_DDC	LEN_EDID	MODE	EN_BACK	INTV_CLK	CLR_PTR	CLR_UPD
$F01F	DDC_ADDR1	$00H	W	VALID_3	VALID_2	VALID_1	-	ADDR_3	ADDR_2	ADDR_1	-
Interrupt Source Control Registers											
Addr.	**Name**	**Init.**	**R/W**	**Bit7**	**Bit6**	**Bit5**	**Bit4**	**Bit3**	**Bit2**	**Bit1**	**Bit0**
$F020	INT_SRC	$00H	R	-	-	INT_IIC0	INT_EXT	-	-	INT_IIC1	INT_HV
External Interrupt Control Registers											
Addr.	**Name**	**Init.**	**R/W**	**Bit7**	**Bit6**	**Bit5**	**Bit4**	**Bit3**	**Bit2**	**Bit1**	**Bit0**
$F021	INTEXT_FLG	$00H	R	-	-	-	-	-	-	INTE1	INTE0
	INTEXT_CLR	-	W	-	-	-	-	-	-	CLR_INTE1	CLR_INTE0
$F022	INTEXT_EN	$00H	W	-	-	INTE1_EDG	INTE0_EDG	-	-	INTE1	INTE0
Sync Processor Interrupt Control Registers											
Addr.	**Name**	**Init.**	**R/W**	**Bit7**	**Bit6**	**Bit5**	**Bit4**	**Bit3**	**Bit2**	**Bit1**	**Bit0**
$F023	INTHV_FLG	$00H	R	INT_H	INT_V	-	-	-	INT_HP	INT_VP	INT_FM
	INTHV_CLR	-	W	INT_H	INT_V	-	-	-	INT_HP	INT_VP	INT_FM
$F024	INTHV_EN	$00H	R/W	INT_H	INT_V	-	-	-	INT_HP	INT_VP	INT_FM
Sync Processor Interrupt Control Registers											
Addr.	**Name**	**Init.**	**R/W**	**Bit7**	**Bit6**	**Bit5**	**Bit4**	**Bit3**	**Bit2**	**Bit1**	**Bit0**
$F025	SYNC_REG	$00H	R/W	EN_FRUN	AUTO_FLT	EN_SOG	EN_CLMP	EN_PAT	EN_HALH	HALF_SEL	HALF_NOT
$F026	HVO_REG	$00H	R/W	EN_HOUT	EN_VOUT	EN_HRUN	EN_VRUN	EN_INS	SYNC_SEL	HO_POL	VO_POL
$F027	HVI_REG	$E0H	R	SYNC_S1	SYNC_S0	INS_PW	-	H_LVL	V_LVL	H_POL	V_POL
		-	W	SYNC_S1	SYNC_S0	INS_PW	-	-	-	-	-
$F028	HPW_REG	$00H	R	HPW7	HPW6	HPW5	HPW4	HPW3	HPW2	HPW1	HPW0
$F029	HFLT_REG	$FFH	R/W	HFLT7	HFLT6	HFLT5	HFLT4	HFLT3	HFLT2	HFLT1	HFLT0
$F02A	CLMP_REG	$0CH	W	-	-	-	-	EDG	POL	PW1	PW0
$F02B	PAT_LT	$40H	W	PAT_L7	PAT_L6	PAT_L5	PAT_L4	PAT_L3	PAT_L2	PAT_L1	PAT_L0
$F02C	PAT_RT	$40H	W	PAT_R7	PAT_R6	PAT_R5	PAT_R4	PAT_R3	PAT_R2	PAT_R1	PAT_R0
$F02D	PAT_UP	$80H	W	PAT_U7	PAT_U6	PAT_U5	PAT_U4	PAT_U3	PAT_U2	PAT_U1	PAT_U0
$F02E	PAT_DN	$80H	W	PAT_D7	PAT_D6	PAT_D5	PAT_D4	PAT_D3	PAT_D2	PAT_D1	PAT_D0
$F02F	HVCNT_CTL	$00H	W	-	-	-	-	VOV_S1	VOV_S0	HGATE_SRC	HGATE_TM
$F030	HCNT_LB	$00H	R	HCNT7	HCNT6	HCNT5	HCNT4	HCNT3	HCNT2	HCNT1	HCNT0
$F031	HCNT_HB	$00H	R	HCNTOV	-	-	-	HCNT11	HCNT10	HCNT9	HCNT8
$F032	VCNT_LB	$00H	R	VCNT7	VCNT6	VCNT5	VCNT4	VCNT3	VCNT2	VCNT1	VCNT0
$F033	VCNT_HB	$00H	R	VCNTOV	-	VCNT13	VCNT12	VCNT11	VCNT10	VCNT9	VCNT8
$F034	DCNT_LB	$7CH	W	DCNT7	DCNT6	DCNT5	DCNT4	DCNT3	DCNT2	DCNT1	DCNT0
$F035	DCNT_HB	$01H	W	-	-	-	-	-	-	-	DCNT8
$F036	LCNT_LB	$0DH	W	LCNT7	LCNT6	LCNT5	LCNT4	LCNT3	LCNT2	LCNT1	LCNT0
$F037	LCNT_HB	$02H	W	-	-	-	-	-	LCNT10	LCNT9	LCNT8
$F038	MUTE_CTL	$C0H	W	UPD_HT	AUTO_UPD	HS_ACT	VS_ACT	DIFF_CNT1	DIFF_CNT0	DIFF_VAL1	DIFF_VAL0

System Registers （Continued）

I²C Bus Port-0 Control Registers (PB4,PB5)											
Addr.	**Name**	**Init.**	**R/W**	**Bit7**	**Bit6**	**Bit5**	**Bit4**	**Bit3**	**Bit2**	**Bit1**	**Bit0**
$F039	IIC0_CFG	$00H	R/W	PRENACK	SEND_ACK	STOP	RESTART	RB1	RB0	MASTER	WAIT
$F03A	IIC0_STATUS	$00H	R	WRITE	READ	TXDATA_FULL	TX_FULL	RXDATA_NULL	RX_NULL	BUS_START	BUS_STOP
$F03B	INTIIC0_EN	$00H	R/W	INTA	INTTX	INTRX	INTNAK	INTLOST	-	-	-
$F03C	INTIIC0_FLG	$00H	R	INTA	INTTX	INTRX	INTNAK	INTLOST	-	-	-
		-	W	-	-	-	-	-	-	START_GEN	STOP_GEN
$F03D	INTIIC0_CLR	$00H	W	INTA	INTTX	INTRX	INTNAK	INTLOST	CLR_TX_FIFO	CLR_FIFO	-
$F03E	IIC0_TXDATA	$00H	W	TXDATA7	TXDATA6	TXDATA5	TXDATA4	TXDATA3	TXDATA2	TXDATA1	TXDATA0
$F03F	IIC0_RXDATA	$00H	R	RXDATA7	RXDATA6	RXDATA5	RXDATA4	RXDATA3	RXDATA2	RXDATA1	RXDATA0
$F040	IIC0_ADDR	$B0H	R/W	ADDR7	ADDR6	ADDR5	ADDR4	ADDR3	ADDR2	ADDR1	ENIIC0
I²C Bus Port-1 Control Registers (PB6,PB7)											
Addr.	**Name**	**Init.**	**R/W**	**Bit7**	**Bit6**	**Bit5**	**Bit4**	**Bit3**	**Bit2**	**Bit1**	**Bit0**
$F041	IIC1_CFG	$00H	R/W	PRENACK	SEND_ACK	STOP	RESTART	RB1	RB0	MASTER	WAIT
$F042	IIC1_STATUS	$00H	R	WRITE	READ	TXDATA_NULL	TX_NULL	RXDATA_NULL	RX_NULL	START	STOP
$F043	INTIIC1_EN	$00H	R/W	INTA	INTTX	INTRX	INTNAK	INTLOST	-	-	-
$F044	INTIIC1_FLG	$00H	R	INTA	INTTX	INTRX	INTNAK	INTLOST	-	-	-
		-	W	-	-	-	-	-	-	START_GEN	STOP_GEN
$F045	INTIIC1_CLR	$00H	W	INTA	INTTX	INTRX	INTNAK	INTLOST	CLR_TX_FIFO	CLR_FIFO	-
$F046	IIC1_TXDATA	$00H	W	TXDATA7	TXDATA6	TXDATA5	TXDATA4	TXDATA3	TXDATA2	TXDATA1	TXDATA0
$F047	IIC1_RXDATA	$00H	R	RXDATA7	RXDATA6	RXDATA5	RXDATA4	RXDATA3	RXDATA2	RXDATA1	RXDATA0
$F048	IIC1_ADDR	$B0H	R/W	ADDR7	ADDR6	ADDR5	ADDR4	ADDR3	ADDR2	ADDR1	ENIIC1
Flash Memory Control Registers											
Addr.	**Name**	**Init.**	**R/W**	**Bit7**	**Bit6**	**Bit5**	**Bit4**	**Bit3**	**Bit2**	**Bit1**	**Bit0**
$F049	ISP_REG	$00H	R	-	-	-	-	-	-	ISP_FLG	ISP_CH
$F04A	FLASH_BUF	$FFH	R/W	BUF7	BUF6	BUF5	BUF4	BUF3	BUF2	BUF1	BUF0

*Note: The flash memory control registers are used for ISP function, users don't need to care for these. If you try to write these registers may cause some unexpected condition.

Section-3 Micro-Processor F8031

3-1 Features of F8031

- Intel 8031 architecture
- 8-Bit CPU optimized for control applications
- Extensive Boolean processing capabilities
- Maximum 64K External Program Memory ability
- Maximum 64K External Data Memory ability
- 256 Bytes of on-chip Data RAM
- 32 bidirectional and individually addressable I/O lines
- Two 16-bit timer/counter
- Fully duplex UART
- 5-vector interrupt structure with two programmable priority levels

3-2 General Description

The F8031 is an 8-bit microprocessor optimized for control applications. Byte-processing and numerical operations on small data strutures are facilitated by a variety of fast addressing modes for Internal RAM. The instruction set provides serveral byte instructions including multiply and divide instructions. In addition, serveral bit oriented instructions are also provided. This allows direct bit manipulation and testing in control and logic systems that require Boolean processing.

3-3 Special Function Registers（SFRs）

The F8031 has a total of 21 SFR's, as shown in the figure below --- **SFR Map for F8031**. Note that not all the addresses are occupied by SFR's. The unoccupied addresses are not implemented and should not be used by the customer. Read access from these unoccupied locations will return unpredictable data, while write accesses will have no effect on the chip.

SFR Map for F8031									
F8H									FFH
F0H	B								F7H
E8H									EFH
E0H	ACC								E7H
D8H									DFH
D0H	PSW								D7H
C8H									CFH
C0H									C7H
B8H	IP								BFH
B0H	P3								B7H
A8H	IE								AFH
A0H	P2								A7H
98H	SCON	SBUF							9FH
90H	P1								97H
88H	TCON	TMOD	TL0	TL1	TH0	TH1			8FH
80H	P0	SP	DPL	DPH				PCON	87H
✧ Note: SFR's in marked column are bit addressable.									

A brief description of the SFR's now follows

3-3.1 Accumulator

ACC is the accumulator register used for most of the arithmetic and logical instructions.

3-3.2 B Register

The B register is an SFR which is used primarily in the multiply and divide instructions. It can also be used as a temporary scratch pad register for the other instructions.

3-3.3 Program Status Word (PSW)

The PSW is the register that holds information ahout the status of the Accumulator, the selected register banks and other information. This register is described in details in the following figure:

PSW – Program Status Word Register		
B7	CY	Carry flag
B6	AC	Auxiliary Carry flag(for BCD operations)
B5	F0	Flag 0(Available to the user for general purposes)
B4	RS1	Register Bank select control bit 1 & 0 Set/cleared by software to determine working bank. (RS1,RS0): (00) – Bank 0 ⇔ Address ➨ (00H ~ 07H) (01) – Bank 1 ⇔ Address ➨ (08H ~ 0FH) (10) – Bank 2 ⇔ Address ➨ (10H ~ 17H) (11) – Bank 3 ⇔ Address ➨ (18H ~ 1FH)
B3	RS0	
B2	OV	Overflow Flag
B1	X	User definable flag
B0	P	Parity Flag Set/Cleared by hardware each instruction cycle to indicate an odd/even number of “one” bit I the Accumlator, i.e., even parity.

3-3.4 Stack Pointer

The Stack Pointer is an 8-bit wide register that is used to point to the top of the stack where addresses are stored. After a reset, the stack pointer is initialized to 07H, and so the stack begins at 08H. However the stack can reside at any location in the Internal RAM and stack pointer can be programmed to suit the user’s needs.

3-3.5 Data Pointer

The Data Pointer (DPTR) consists of a high byte (DPH) and a low byte (DPL). Its intended function is to hold a 16-bit address. It may be manipulated as a 16-bit register or as two independent 8-bit registers.

3-3.6 Port 0,1,2,3

The four ports have four SFR’s associated with them. Data to be brought out onto the port pins is written to the latches.

3-3.7 Serial Data Buffer

The Serial Data Buffer is actually two separate registers, a transmit buffer and a receive buffer register. When data is moved to SBUF, it goes to the transmit buffer where it is held for srial transmission. (Moving a byte to SBUF is what initiates the transmission.) When data is moved from SBUF, it comes from the receive buffer.

3-3.8 Timer Registers

The 8031 has two 16-bit timers, Timer/Counter 0 and Timer/Counter 1. The TH0, TL0 and TH1, TL1 register pairs are the 16-bit counting registers for the two timer/counter respectively.

3-3.9 Control Registers

The SFR’s TCON, TMOD, SCON, IE, IP and PCON are the registers, which contain the control and status bits for the Timer/Counter, the Serial Port and the Interrupt system.

✧ ***For more details please refers to the MCS-51 Programmer’s Guide and Data Sheet of INTEL MCS-51 family.***

3-3.10 Port Structure and Operation

All four ports in the 8031 are bidirectional. Each consists of a latch (SFR's P0 through P3), an output driver, and input buffer. The output drivers of Port 0 and 2, and the input buffers of Port 0, are used in accesses to external memory. In this application, Port 0 outputs the low byte of the external memory address, time multiplexed with the byte being written or read. Port 2 oututs the high byte of the external memory address when the address is 16 bits wide. Otherwise the Port 2 pins continue to emit the P2 SFR content.

All the Port 3 pins are multifunctional. They are not only port pins, but also serve the functions of various special features as listed on the following table:

Alternate Function of Port 3			
Port Pin	Alternate Function	Assigned Function in Our System	
P3.7	RD(external Data Memory read strobe)	Internal signal of MCU	**P3.7 must be held at "1"**
P3.6	WR(external Data Memory write strobe)	Internal signal of MCU	**P3.6 must be held at "1"**
P3.5	T1(Timer/Counter 1 external pin)	P3.5/T1 as I/O Pin	User defined
P3.4	T0(Timer/Counter 0 external pin)	P3.4/T0 as I/O Pin	User defined
P3.3	INT1(external interrupt 1)	Internal signal of MCU	**P3.3 must be held at "1", INT1 is Low Level Triggered**
P3.2	INT0(external interrupt 0)	Internal signal of MCU	**P3.2 must be held at "1", INT0 is Low Level Triggered**
P3.1	TXD(serial output port)	P3.1/TXD as I/O Pin	User defined
P3.0	RXD(serial input port)	P3.0/RXD as I/O Pin	User defined

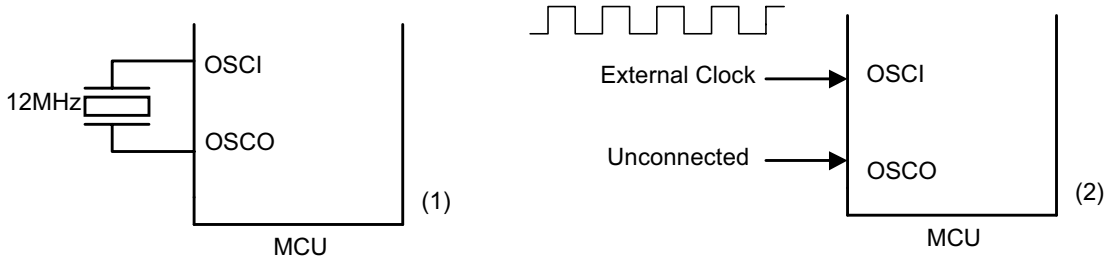
✧ **In order to activate the alternate functions correctly, the corresponding bit latch must be held at value 1.** If this is not done then the corresponding port pin is stuck at 0, and external or internal inputs will have no effect on the pin value.

P10 and P11 are used for bank switch function of the program memory, and you need to pay more attention if you try to control the P10/P11 directly in your program.

Section-4 Oscillator(OSC)

This block generates the system timing and control signal to be supplied to the on-chip peripherals. A quartz crystal or an external clock signal, which will be provided to the OSCI pin to generate the system timing. It generates a 12 MHz system clock. Although internal circuits include a feedback resister and capacitor, users can externally add these components for proper operating. The typical clock frequency is 12MHz. Different frequencies will affect the operation of those on-chip peripherals whose operating frequency is based on the system clock.

In order to speedup the CPU operating clock., based on the 12MHz clock, there is an internal PLL circuit to generate a 24MHz clock to the CPU.



Oscillator Connections

The duty cycle of the OSC output waveform could not be less than 45% for the other circuit application.

Section-5 Reset

There are totally four MCU Reset Sources,
- External RESET Pin
- Low-Voltage Reset
- Watch-Dog Timer Reset
- ISP Reset

5-1 External RSTB Pin

The External Reset, **RSTB** pin is a low active external input signal. The MCU will generate internal system reset when the pin level of the External Reset is less than the lower-threshold voltage $V_{LT(RST)}$ and its pulse width larger than ***64 OSC clock cycles*** (64 t_{OSC}). The reset cycle will end after ***64 OSC clock cycles*** (64 t_{OSC}) when the RESET pin level is larger than the upper-threshold voltage $V_{UT(RST)}$.

5-2 Low-Voltage Reset (LVR) and Power-On Reset (POR)

The Low-Voltage Reset (LVR) Circuit monitors the power input of the MCU. The MCU will generate internal LVR reset when the power level is less than V_{LVR}. The **POR** reset cycle will end will after 2^{16} **OSC Clock pulse** when the power level is larger than voltage V_{LVR}.

5-3 Watch-Dog Timer Reset

This MCU implements a Watch-Dog timer reset to avoid system stop or malfunction. The clock source of the WDT is from the 12MHz on-chip oscillator. The watch-dog timer's interval is about ***0.5 second***. The watch-dog timer must be cleared every 0.5 second when the software is in normal operation sequence, otherwise the watch-dof timer will overflow and causes a system reset. The watch-dog timer is cleared and enabled after the system is reset, and cannot be disabled by the software. Users can clear the watch-dog timer by writing a #55H into the CLRWDT register.

```
MOV     A,#55H
MOV     DPTR,#CLRWDT
MOVX    @DPTR,A
```

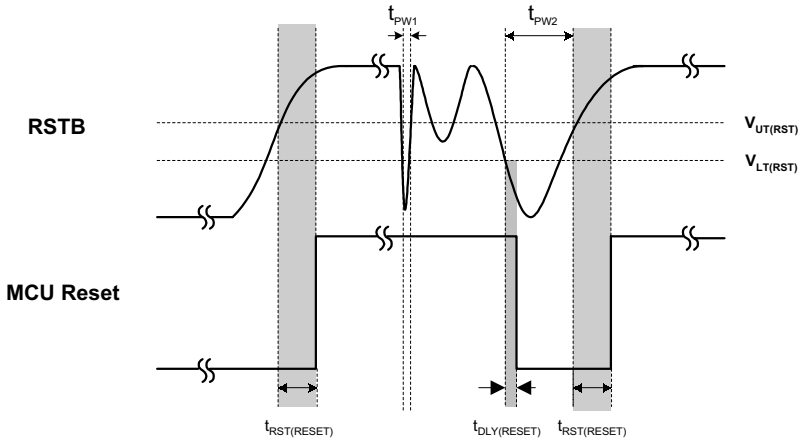
Where,
CLRWDT is an Assembler constant symbol, which is defined as the address value of the register **CLRWDT** in system register file of this MCU.

5-4 ISP Reset

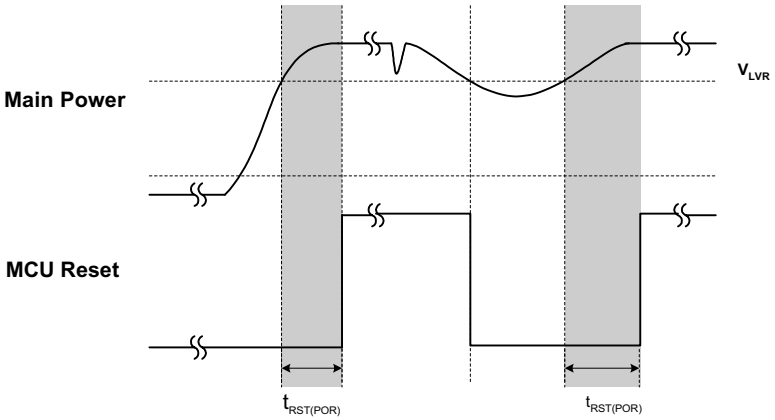
The ISP Reset will be generated when the built-in ISP state machine recognizes the special ISP Reset Pattern. It resets the CPU only, and then enters the ISP mode from the normal operation mode.

Affection of Reset

Function Circuit / Reset Sources	CPU	Pin Configuations	ISP Recognizing
RSTB Reset	✓	✓	✓
LVR Rest	✓	✓	✓
WDT Reset	✓	✓	✓
ISP Reset	✓	✗	✗
Where, ✓ = reset ✗ = no effect			
Note: Please don't force the I^2C bus low, otherwise the ISP pattern can't be generated.			



External Reset(RSTB)



Low-Voltage Reset (LVR)

Section-6 Input/Output Ports

6-1 Port-A Configuration

Pin Designation	Function	I/O	Circuit Structure		Control Bits	
					RDPA_7	EN_PWM9
PA7*/PWM9*	PA7*	I/O	Open-Drain	Shown in Fig.6-1	-	0
	PWM9*	O	Open-Drain		X	1
Designation	**Function**	**I/O**	**Circuit Structure**		**Control Bits**	
					RDPA_6	**EN_PWM8**
PA6*/PWM8*	PA6*	I/O	Open-Drain	Shown in Fig.6-1	-	0
	PWM8*	O	Open-Drain		X	1
Designation	**Function**	**I/O**	**Circuit Structure**		**Control Bits**	
					RDPA_5	**EN_PWM7**
PA5*/PWM7*	PA5*	I/O	Open-Drain	Shown in Fig.6-1	-	0
	PWM7*	O	Open-Drain		X	1
Designation	**Function**	**I/O**	**Circuit Structure**		**Control Bits**	
					RDPA_4	**EN_PWM6**
PA4*/PWM6*	PA4*	I/O	Open-Drain	Shown in Fig.6-1	-	0
	PWM6*	O	Open-Drain		X	1

Designation	Function	I/O	Circuit Structure		Control Bits	
					RDPA_3	EN_PWM5
PA3/PWM5	PA3	I	Weakly Pull High	Shown in Fig.6-5	1	0
		O	Push-Pull		0	0
	PWM5	O	Push-Pull		X	1
Designation	**Function**	**I/O**	**Circuit Structure**		**Control Bits**	
					RDPA_2	**EN_PWM4**
PA2/PWM4	PA2	I	Weakly Pull High	Shown in Fig.6-5	1	0
		O	Push-Pull		0	0
	PWM4	O	Push-Pull		X	1
Designation	**Function**	**I/O**	**Circuit Structure**		**Control Bits**	
					RDPA_1	**EN_PWM3**
PA1/PWM3	PA1	I	Weakly Pull High	Shown in Fig.6-5	1	0
		O	Push-Pull		0	0
	PWM3	O	Push-Pull		X	1
Designation	**Function**	**I/O**	**Circuit Structure**		**Control Bits**	
					RDPA_0	**EN_PWM2**
PA0/PWM2	PA0	I	Weakly Pull High	Shown in Fig.6-5	1	0
		O	Push-Pull		0	0
	PWM2	O	Push-Pull		X	1

6-2 Port-B Configuration

Designation	Function	I/O	Circuit Structure		Control Bits	
					RDPB_7	EN_IIC1
PB7*/SDA1*	PB7*	I/O	Open-Drain	Shown in Fig.6-1	-	0
	SDA1*	I/O	Open-Drain		X	1
Designation	**Function**	**I/O**	**Circuit Structure**		**Control Bits**	
					RDPB_6	**EN_IIC1**
PB6*/SCL1*	PB6*	I/O	Open-Drain	Shown in Fig.6-1	-	0
	SCL1*	I/O	Open-Drain		X	1
Designation	**Function**	**I/O**	**Circuit Structure**		**Control Bits**	
					RDPB_5	**EN_IIC0**
PB5*/SDA0*	PB5*	I/O	Open-Drain	Shown in Fig.6-1	-	0
	SDA0*	I/O	Open-Drain		X	1
Designation	**Function**	**I/O**	**Circuit Structure**		**Control Bits**	
					RDPB_4	**EN_IIC0**
PB4*/SCL0*	PB4*	I/O	Open-Drain	Shown in Fig.6-1	-	0
	SCL0*	I/O	Open-Drain		X	1

Designation	Function	I/O	Circuit Structure		Control Bits	
					RDPB_3	EN_ADC3
PB3/ADC3 /INTE1	PB3	I	Weakly Pull High	Shown in Fig.6-4	1	0
		O	Push-Pull		0	0
	ADC3	I	Hi-Z		X	1
Designation	**Function**	**I/O**	**Circuit Structure**		**Control Bits**	
					RDPB_2	**EN_ADC2**
PB2/ADC2 /INTE0	PB2	I	Weakly Pull High	Shown in Fig.6-4	1	0
		O	Push-Pull		0	0
	ADC2	I	Hi-Z		X	1
Designation	**Function**	**I/O**	**Circuit Structure**		**Control Bits**	
					RDPB_1	**EN_ADC1**
PB1/ADC1	PB1	I	Weakly Pull High	Shown in Fig.6-4	1	0
		O	Push-Pull		0	0
	ADC1	I	Hi-Z		X	1
Designation	**Function**	**I/O**	**Circuit Structure**		**Control Bits**	
					RDPB_0	**EN_ADC0**
PB0/ADC0	PB0	I	Weakly Pull High	Shown in Fig.6-4	1	0
		O	Push-Pull		0	0
	ADC0	I	Hi-Z		X	1

6-3 Port-C Configuration

Designation	Function	I/O	Circuit Structure		Control Bit(s)	
					RDPC_B7	
PC7	PC7	I	Weakly Pull High	Shown in Fig.6-5	1	
		O	Push-Pull		0	
Designation	**Function**	**I/O**	**Circuit Structure**		**Control Bit(s)**	
					RDPC_B6	
PC6	PC6	I	Weakly Pull High	Shown in Fig.6-5	1	
		O	Push-Pull		0	
Designation	**Function**	**I/O**	**Circuit Structure**		**Control Bit(s)**	
					RDPC_B5	**EN_PAT**
PC5/PATTO	PC5	I	Weakly Pull High	Shown in Fig.6-5	1	0
		O	Push-Pull		0	0
	PATTO	O	Push-Pull		X	1
Designation	**Function**	**I/O**	**Circuit Structure**		**Control Bit(s)**	
					RDPC_B4	**EN_PWM1**
PC4/PWM1	PC4	I	Weakly Pull High	Shown in Fig.6-5	1	0
		O	Push-Pull		0	0
	PWM1	O	Push-Pull		X	1

Designation	Function	I/O	Circuit Structure		Control Bit(s)	
					RDPC_3	EN_PWM0
PC3/PWM0	PC3	I	Weakly Pull High	Shown in Fig.6-5	1	0
		O	Push-Pull		0	0
	PWM0	O	Push-Pull		X	1
Designation	**Function**	**I/O**	**Circuit Structure**		**Control Bit(s)**	
					RDPC_2	**EN_SOG**
PC2/SOGI	PC2	I	Weakly Pull High	Shown in Fig.6-5	1	0
		O	Push-Pull		0	0
	SOGI	I	Weakly Pull High		X	1
Designation	**Function**	**I/O**	**Circuit Structure**		**Control Bit(s)**	
					RDPC_1	
PC1*	PC1*	I/O	Open-Drain	Shown in Fig. 6-2	-	
Designation	**Function**	**I/O**	**Circuit Structure**		**Control Bit(s)**	
					RDPC_0	
PC0*	PC0*	I/O	Open-Drain	Shown in Fig.6-2	-	

6-4 Port-D Configuration

Designation	Function		Circuit Structure		Control Bit(s)	
					RDPD_6	
PD6	PD6	I	Weakly Pull High	Shown in Fig.6-3	1	
		O	Push-Pull		0	
Designation	**Function**		**Circuit Structure**		**Control Bit(s)**	
					RDPD_5	**EN_CLMP**
PD5/CLMPO	PD5	I	Weakly Pull High	Shown in Fig.6-5	1	0
		O	Push-Pull		0	0
	CLMPO	O	Push-Pull		X	1
Designation	**Function**		**Circuit Structure**		**Control Bit(s)**	
					RDPD_B4	**EN_HALF**
PD4/HALFI	PD4	I	Weakly Pull High	Shown in Fig.6-6	1	0
		O	Push-Pull		0	0
	HALFI	I	Weakly Pull High		X	1

Designation	Function		Circuit Structure		Control Bit(s)	
					RDPD_B5	EN_HALF
PD3/HALFO	PD3	I	Weakly Pull High	Shown in Fig.6-7	1	0
		O	Push-Pull		0	0
	HALFO	O	Push-Pull		X	1
Designation	**Function**		**Circuit Structure**		**Control Bit(s)**	
					RDPD_2	**EN_VOUT**
PD2/VSYNCO	PD2	I	Weakly Pull High	Shown in Fig.6-5	1	0
		O	Push-Pull		0	0
	VSYNCO	O	Push-Pull		X	1
Designation	**Function**		**Circuit Structure**		**Control Bit(s)**	
					RDPD_1	**EN_HOUT**
PD1/HSYNCO	PD1	I	Weakly Pull High	Shown in Fig.6-5	1	0
		O	Push-Pull		0	0
	HSYNCO	O	Push-Pull		X	1
Designation	**Function**		**Circuit Structure**		**Control Bit(s)**	
					RDPD_B0	
PD0	PD0	I	Weakly Pull High	Shown in Fig.6-3	1	
		O	Push-Pull		0	

6-5 Port-E Configuration（Only available in PLCC package）

Designation	Function		Circuit Structure		Control Bit(s)
					RDPE_1
PE1	PE1	I	Weakly Pull High	Shown in Fig.6-3	1
		O	Push-Pull		0
Designation	**Function**		**Circuit Structure**		**Control Bit(s)**
					RDPE_0
PE0	PE0	I	Weakly Pull High	Shown in Fig.6-3	1
		O	Push-Pull		0

6-6 Port-3 Configuration:

Port-3 is a general purpose I/O Port of the F8031. Its port structure is refered to Fig.6-8. Each bi-directional I/O pin may be bit programmed as an input or an output port without using software to control the data direction register. When PORT-3 works as an output, the data to be output is latched to the port data register and outputted to the pin. PORT3 pins that have '1's written to them are pulled HIGH by the internal PMOS pull-ups. In this state they can be used as an input. The input signal can be read.

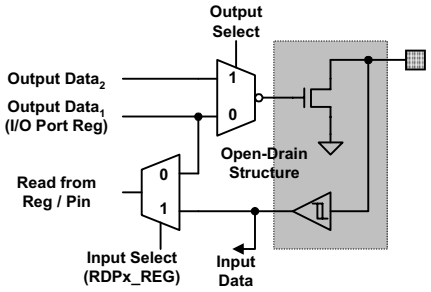


Fig.6-1

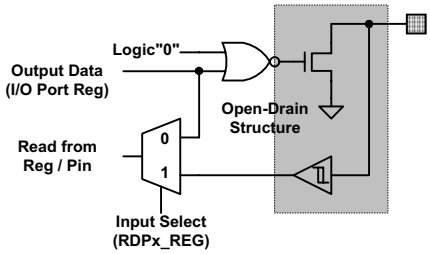


Fig.6-2

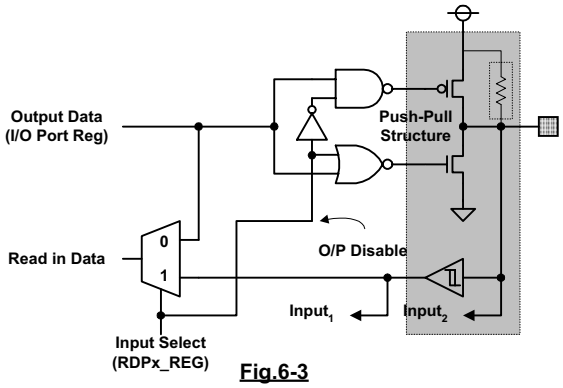


Fig.6-3

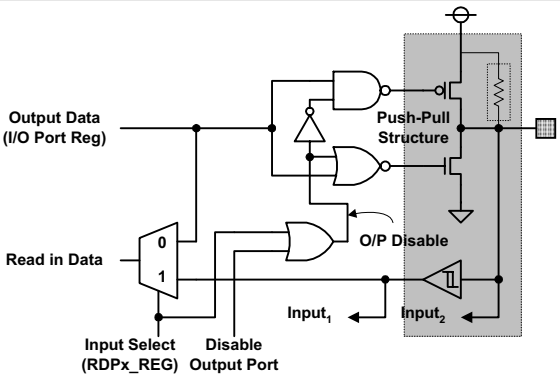


Fig.6-4

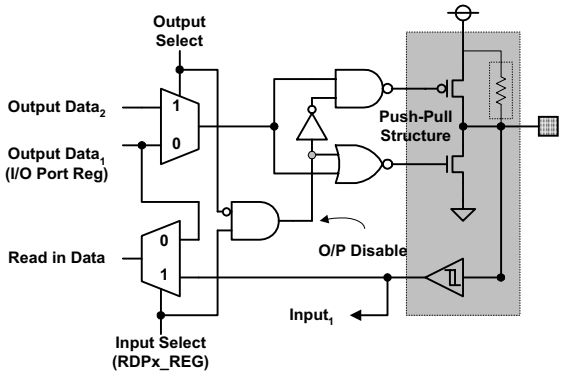


Fig.6-5

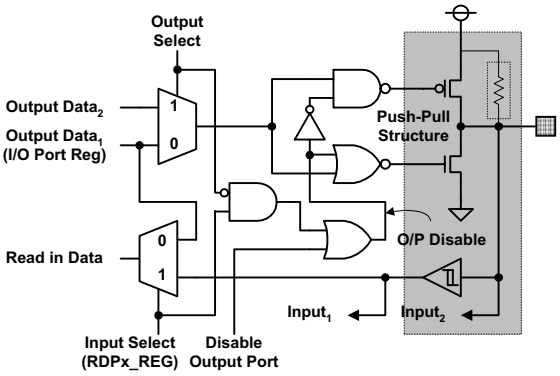


Fig.6-6

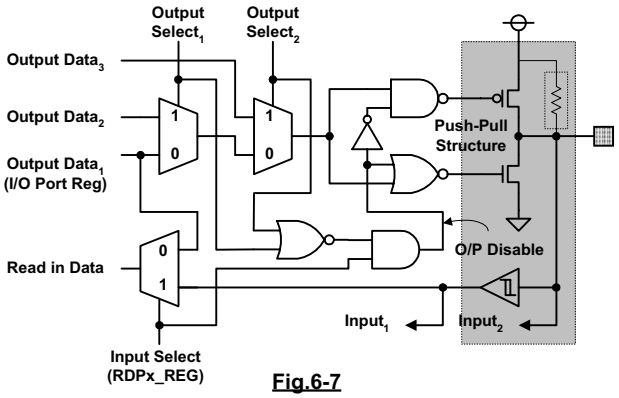

Output Select1
Output Select2
Output Data3
Output Data2
Output Data1 (I/O Port Reg)
Read in Data
Input Select (RDPx_REG)
Push-Pull Structure
O/P Disable
Input1
Input2

Fig.6-7

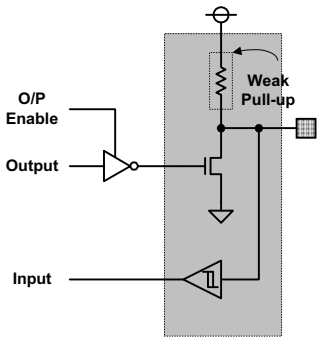

O/P Enable
Output
Input
Weak Pull-up

Fig.6-8

Section-7 Interrupts

7-1 Inerrupt Overview of the 8031

The F8031 provides 5 interrupt sources: 2 external interrupts, 2 timer interrupts, and a serial port interrupt. What follows is an overview of the interrupt structure for the F8031.

7-1.1 Interrupt Enables

Each of the interrupt sources can be individually enabled or disabled by setting or clearing a bit in the SFR named IE (Interrupt Enable). This register also contains a global disable bit, which can be cleared to disable all interrupts at once. The following figure shows the IE register for F8031

IE (Interrupt Enable) Register in the F8031		
B7	EA	Disable all interrupts. If EA=0, no any interrupts will be acknowledged. If EA=1, each interrupt source is individually enabled or disabled by setting or clearing its enable bit.
B6	X	Unused
B5	X	Unused
B4	ES	Serial Port Interrupt enable bit
B3	ET1	Timer 1 Overflow Interrupt enable bit
B2	EX1	External Interrupt 1 enable bit
B1	ET0	Timer 0 Overflow Interrupt enable bit
B0	EX0	External Interrupt 0 enable bit
✧ Enable bit = 1, enables the interrupt ✧ Enable bit = 0, disables the interrupt		

7-1.2 Interrupt Priorities

Each interrupt source can also be individually programmed to one of the two priority levels by setting or clearing a bit in the SFR named IP (Interrupt Priority). The following figure shows the IP register in F8031.

IP (Interrupt Priority) Register in the F8031		
B7	X	Unused
B6	X	Unused
B5	X	Unused
B4	PS	Serial Port Interrupt priority bit
B3	PT1	Timer 1 Overflow Interrupt priority bit
B2	PX1	External Interrupt 1 priority bit
B1	PT0	Timer 0 Overflow Interrupt priority bit
B0	PX0	External Interrupt 0 priority bit
✧ Priority bit = 1, assign high priority ✧ Priority bit = 0, assign low priority		

A low-priority interrupt can be interrupted by a high-priority interrupt, but cannot be interrupted by another low-priority interrupt. A high-priority interrupt cannot be interrupted by any other interrupt source.
If two interrupt requests of different priority levels are received simultaneously, the request of higher priority level is serviced. If interrupt requests of the same priority level are received simultaneously, an internal polling sequence determines which request is serviced first. Thus within each priority level there is a second priority structure determined by software polling sequence.
In operation, all the interrupt flags are latched into the interrupt control system every machine cycle. The samples are polled during the following machine cycle. If the flag for an enabled interrupt is found to be 1, the interrupt system generates an LCALL to the appropriate location in Program Memory, unless some other conditions block an interrupt, among them that an interrupt of equal or higher priority level is already in progress.
The hardware-generated LCALL accesses the contents of the Program Counter to push onto the stack, and reload the PC with the beginning address of the service routine. As previously noted, the service routine for each interrupt begins at a fixed location.
Only the Program Counter is automatically pushed onto the stack, not the PSW or any other register. Having only the PC to be automatically saved allows the programmer to decide how much time to spend on saving which register. This enhances the interrupt response time, albeit at expense of increasing the programmer's burden of responsibility. As a result, many interrupt functions that are typical in control applications – togglig a port pin, for example, or reloading a timer, or unloading a serial buffer – can often be completed in less time than it takes for other architectures to commence them.

7-2 Interrupt Controller

The system provides 5-vector interrupt structure:
- TF0: Timer/Counter 0 Overflow Interrupt
- TF1: Timer/Counter 1 Overflow Interrupt
- RI+TI: UART Interrupts
- INT0:
  - Sync Processor Interrupts
  - I^2C-Bus Port-0 (PB4, PB5) Interrupts
- INT1:
  - External Interrupts: INTE0 & INTE1
  - I^2C-Bus Port-1 (PB6, PB7) Interrupts

These 5 interrupt sources have their own individual interrupt vector addresses. See the table below:

Address	Interrupt Source	Description
0000H	Reset	System Reset
0003H	IE0	External INT0 Interrupt of the uP F8031
000BH	TF0	Timer/Counter 0 Overflow Interrupt of the uP F8031
0013H	IE1	External INT1 Interrupt the of uP F8031
001BH	TF1	Timer/Counter 1 Overflow Interrupt of the uP F8031
0023H	RI & TI	UART Transmit interrupt & Receive interrupt of the uP F8031

INT0 and INT1 are extended into the other additional interrupt functions in our system. Because the expansion uses the latched level of the additional sources, a notice must be taken, **users must set the INT0 and INT1 to Low Level Triggered External Interrupt by setting the IT0 and IT1 bits in TCON register of SFR.**

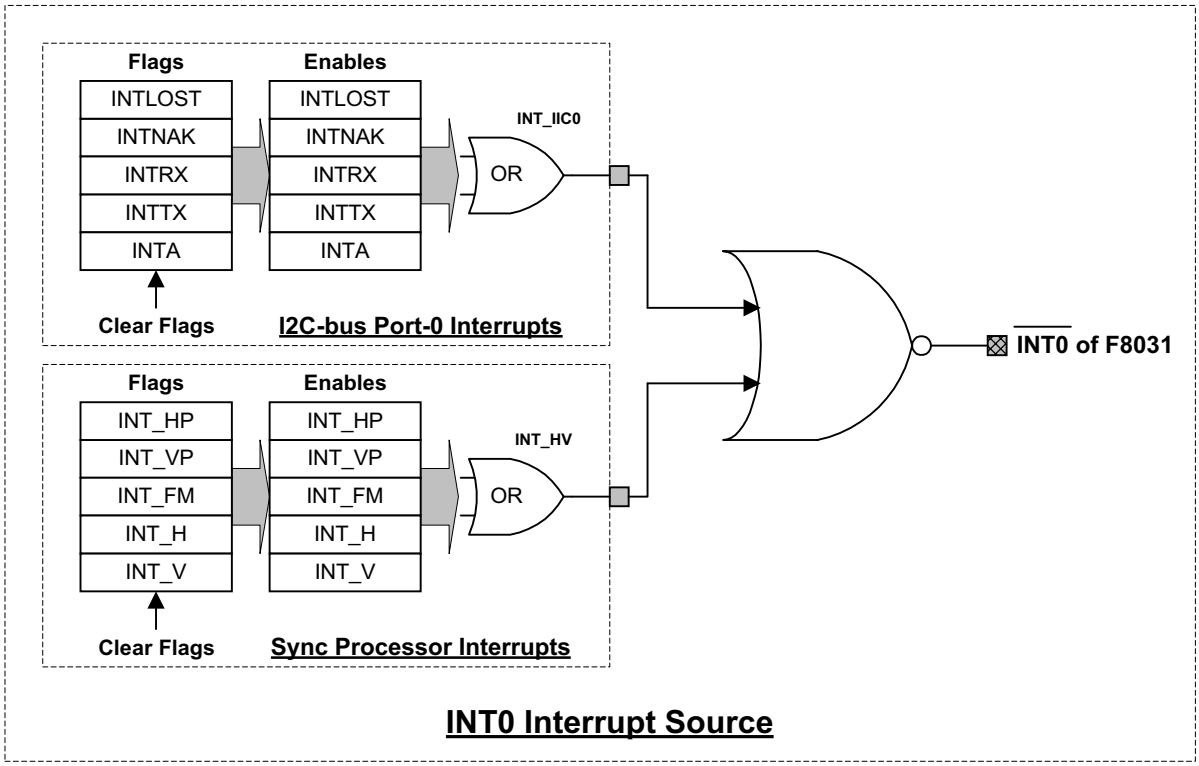
IT0	TCON.0	Interrupt 0 type control bit Set/cleared by software to specify falling edge/low level triggered externl interrupt
IT1	TCON.2	Interrupt 1 type control bit Set/cleared by software to specify falling edge/low level triggered externl interrupt

7-3 Interrupt Sources from INT0 AND INT1

Register	INT_SRC	Interrupt Sources from INT0 AND INT1	
B7	X	-	Unused
B6	X	-	Unused
B5	INT_IIC0	R	1 ➡ INT0 Interrupt request caused by INTIIC0_FLG
B4	INT_EXT	R	1 ➡ INT1 Interrupt request caused by INTEXT_FLG
B3	X	-	Unused
B2	X	-	Unused
B1	INT_IIC1	R	1 ➡ INT1 Interrupt request caused by INTIIC1_FLG
B0	INT_HV	R	1 ➡ INT0 Interrupt request caused by INTHV_FLG

7-3.1 INT0 Interrupt Sources

The INT0, external interrupt 0, are expanded into 2 extra interrupt sources, which are INTIIC0_IRQ and INTHV_IRQ. The following figure shows the detailed structure of the INT0 sources.



INT0 Interrupt Source

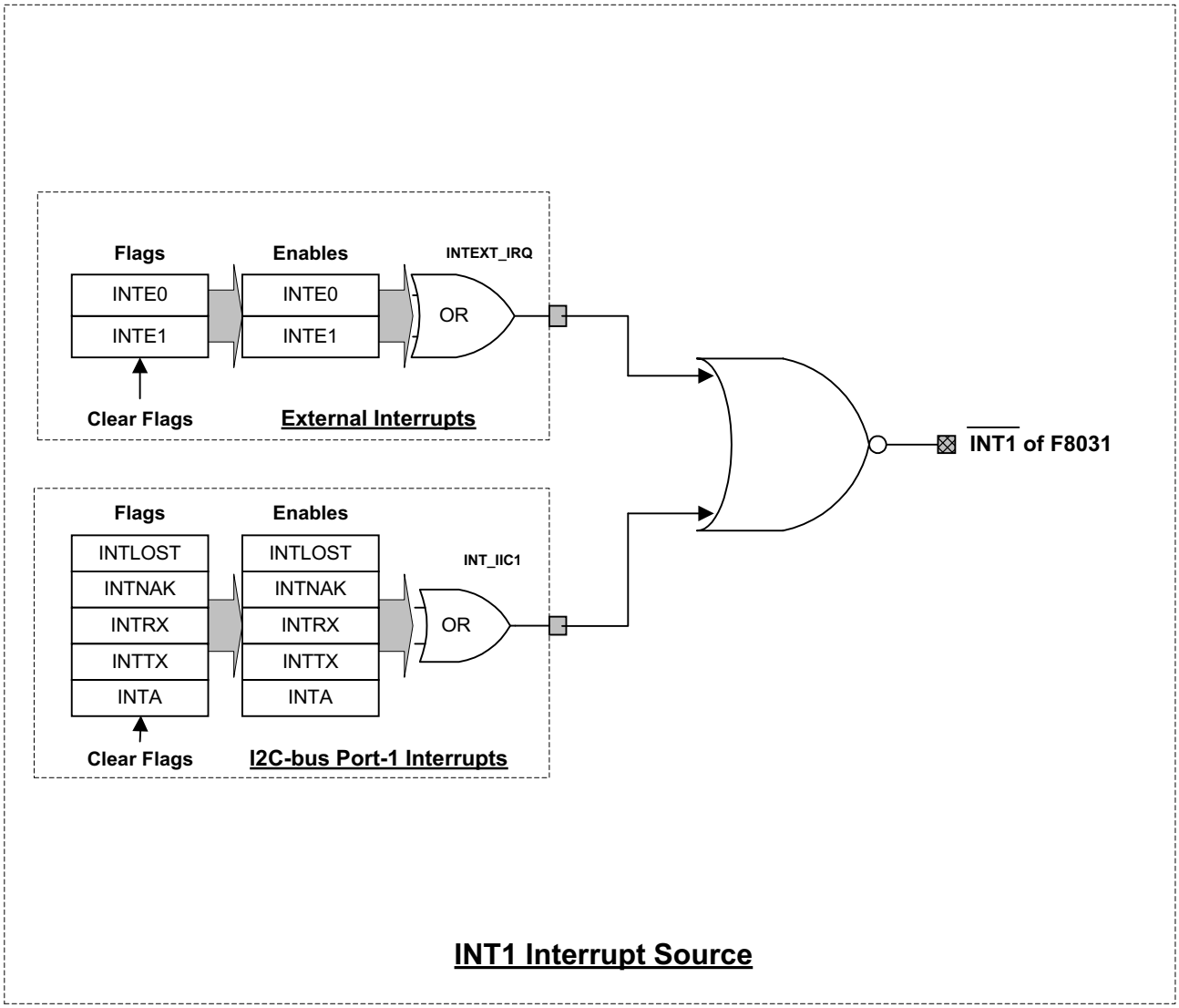
The INTIIC0_IRQ is an interrupt source caused by I²C-bus port0. The INTHV_IRQ interrupt is caused by the sync processor. The detailed descriptions are shown in the following tables.

INTHV_IRQ	Meaning	Action
INT_HP	H-Polarity Change INT	It will be activated when the Input Polarity of Vsync changes.
INT_VP	V-Polarity Change INT	It will be activated when the Input Polarity of Hsync changes.
INT_FM	Fast-Mute INT	It will be activated when the Fast-Mute block detects astable Hsync period.
INT_H	Hsync Edge INT	It will be activated when the Hsync edge is match with the selected trigger edge.
INT_V	Vsync Edge INT	It will be activated when the Vsync edge is match with the selected trigger edge.

INTIIC0_IRQ	Meaning	Action
INTA0	Address Matched INT0	It will be activated in slave mode when the external device calls this I²C-bus port slave address. If this calling address matches the device address, system will generate this interrupt to remind user
INTTX0	Transfer Buffer Empty INT0	It will be activated when transmission buffer is empty in transmission mode.
INTRX0	Receiving Buffer Overflow INT0	It will be activated when new data have store in the data register in receive mode.
INTNAK0	No Acknowledge INT0	In transmission mode, this interrupt will be activated when MCU have sent out one byte data but the external device does not respond an acknowledge bit back to it.
INTLOST0	Arbitration Lost INT0	It will be activated in MASTER mode, if the I²C bus lost the arbitration.

7-3.2 INT1 Interrupt Sources

The INT1, external interrupt source 1, is expanded into two groups, which are INTIIC1_IRQ, and INTEXT_IRQ. The following figure shows the detailed structure of the INT1 sources.



INT1 Interrupt Source

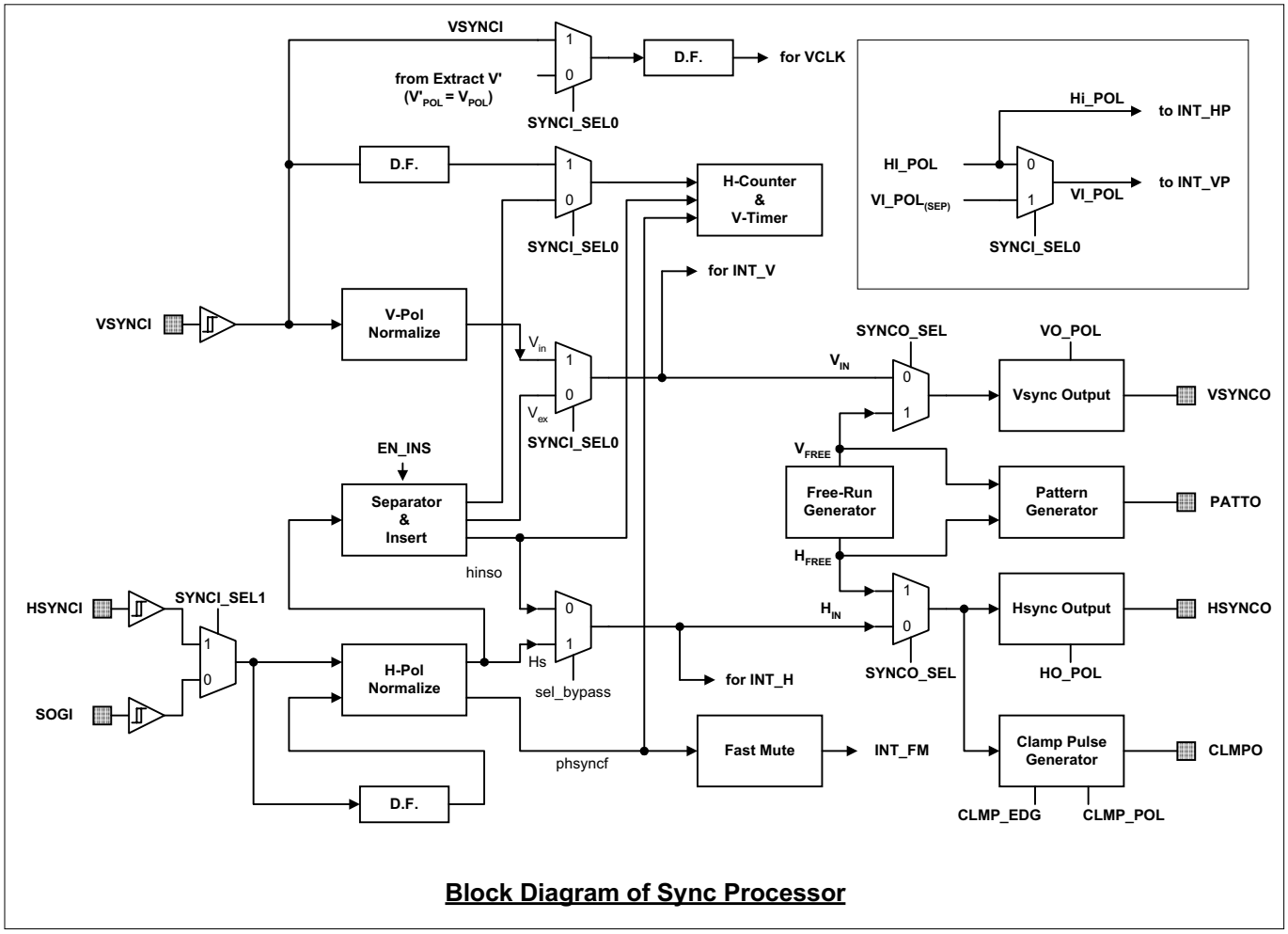
The INTEXT_IRQ is caused by the external interrupt input pins of the INTE0/INTE1, the INTIIC1_IRQ is the interrupt caused by the I²C bus. The more detail descriptions are shown as the below table.

INTIIC1_IRQ	Meaning	Action
INTA1	Address Matched INT1	It will be activated in slave mode when the external device calls this I²C-bus port slave address. If this calling address matches the device address, system will generate this interrupt to remind user
INTTX1	Transfer Buffer Empty INT1	It will be activated when transmission buffer is empty in transmission mode.
INTRX1	Receiving Buffer Overflow INT1	It will be activated when new data have store in the data register in receive mode.
INTNAK1	No Acknowledge INT1	In transmission mode, this interrupt will be activated when MCU have sent out one byte data but the external device does not respond an acknowledge bit back to it.
INTLOST1	Arbitration Lost INT1	It will be activated in MASTER mode, if the I²C bus lost the arbitration.

INTEXT_IRQ	Meaning	Action
INTE0	Edge Triggered External INT Input 0	It will be activated when the resume state is detected.
INTE1	Edge Triggered External INT Input 1	It will be activated when the resume state is detected.

Section-8 Sync Processor

The architecture of the sync processor is shown in **Sync Processor Block Diagram.** The functions of the modules include polarity detection, horizontal frequency counter, vertical frequency counter, and polarity controllable **HSYNCO** and **VSYNCO** outputs of various input sources, such as separate H & V, Composite Sync from HSYNCI, Sync-On-Green, or internal selectable free running H & V pulses. Besides, it also provides the **CLMPO** pulse output to the external video Pre-Amp. The **SYNC_SEL1/0** bit in **SYNC_CTRL** register will determine the type of the input sync sources. All the HSYNCI, and VSYNCI inputs are with internal Schmitt trigger to improve noise immunity.



Block Diagram of Sync Processor

8-1 Sync Input Mode

The video sync signals input from the pins HSYNCI and VSYNCI and SOGI. All the VSYNCI and HSYNCI pins have Schmitt Trigger and filtering process to improve the noise immunity. Any pulse that is shorter than **125ns** will be regarded as a glitch and will be ignored.

SYNCI_SEL1	SYNCI_SEL0	Sync Source
0	-	Composite Sync from SOGI
1	0	Composite Sync from HSYNCI
1	1	Separate Sync from HSYNCI/VSYNCI

8-2 Frequency Calculation

8-2.1 Vsync counter

VCNT_LB/HB, the 14-bit READ ONLY register, contains information of the Vsync frequency. An internal counter counts the numbers of 8us pulse between two VSYNC pulses. When a next VSYNC signal is recognized, the counter is stopped and the VCNT_HB/LB register latches the counter value and then the counter counts from zero again for evaluating the next VSYNC time interval. The counted data can be converted into the time duration between two successive Vsync pulses by times 8us. If no VSYNC is incoming, the counter will overflow and set the VCNTOV bit (in VCNT_HB register) to HIGH. Once the VCNTOV is set to HIGH, it will not change until the next counter cycle is updated. That means the VCNTOV bit will be updated every Vsync Counter cycle. It is necessary for various applications to provide various overflow time intervals. They are selected as shown in the following table.

VOV_SEL1	VOV_SEL0	Time Interval
0	0	32.768ms
0	1	65.536ms
1	0	98.304ms
1	1	131.072ms

8-2.2 Hsync counter

If the **HGATE_SRC** bit is set to Low, the internal counter counts the Hsync pulses between two Vsync pulses. The HCNT_LB/HB control registers contain the numbers of Hsync pulse between two Vsync pulses. These data can determine if the Hsync frequency is valid or not to determine the accurate video mode. The system supports two other options of interval for users to calculate the frequency of Hsync pulses. If users set the HGAT_SRC and the HGATE_TME bits properly, the internal counter counts the Hsync pulses during this system defined time interval. The time interval is defined below:

HGATE_SRC	HGATE_TME	Gate Time
0	-	Vsync Period
1	0	16.384 ms
1	1	32.768 ms

After system reset, this gate interval source will be disabled and the content of **HGATE_SRC** bits are '0'. When this function is disabled, the HCNT_LB/HB counter is working on the VSYNC pulse.

Latching the Hsync counter: The counted value will be latched by the HCNT_HB/LB registers which are updated by Vsync pulse or user's selected time interval. If the counter overflows, the HCNTOV bit (in HCNT_HB register) will be set to HIGH. It will not change until the next counter cycle is updatedt. That means the HCNTOV bit will be updated every Gate cycle of Hsync Counter.

All Counters are with 2-lay content latches for counting sync period/frequency, so user will get the stable counter results even at the latch transient.

8-2.3 Calculation of the H/V SYNC Frequency

Vsync Frequency:

1. Extract the 14-bit Vsync counter data from the VCNT_HB, VCNT_LB control register.
2. The time duration between two Vsync pulse = 14-bit data (VCNT_HB,VCNT_LB)*8 μS
3. The Vsync frequency = 1/(time duration between two Vsync pulses)

Hsync Frequency:

1. Extract the 12-bit Hsync counter data from the HCNT_HB, VCNT_LB control register.

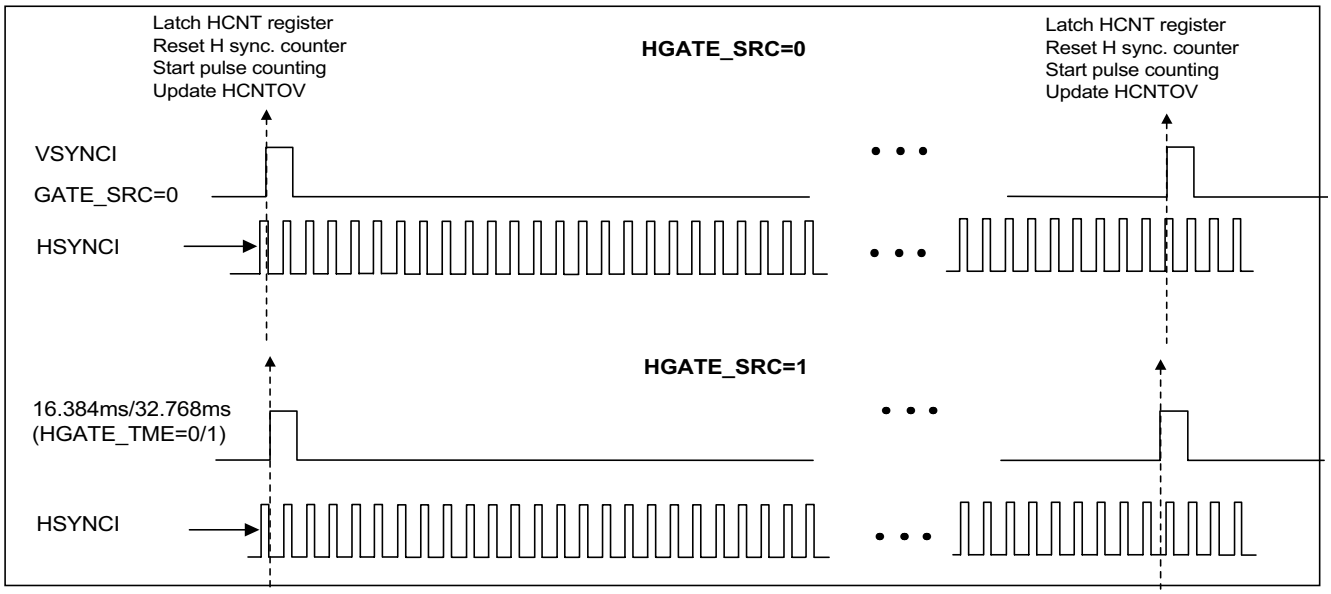
If HGATE=0,

2. The Hsync frequency = 12-bit data (HCNT_HB,HCNT_LB)*(Vsync Frequency)

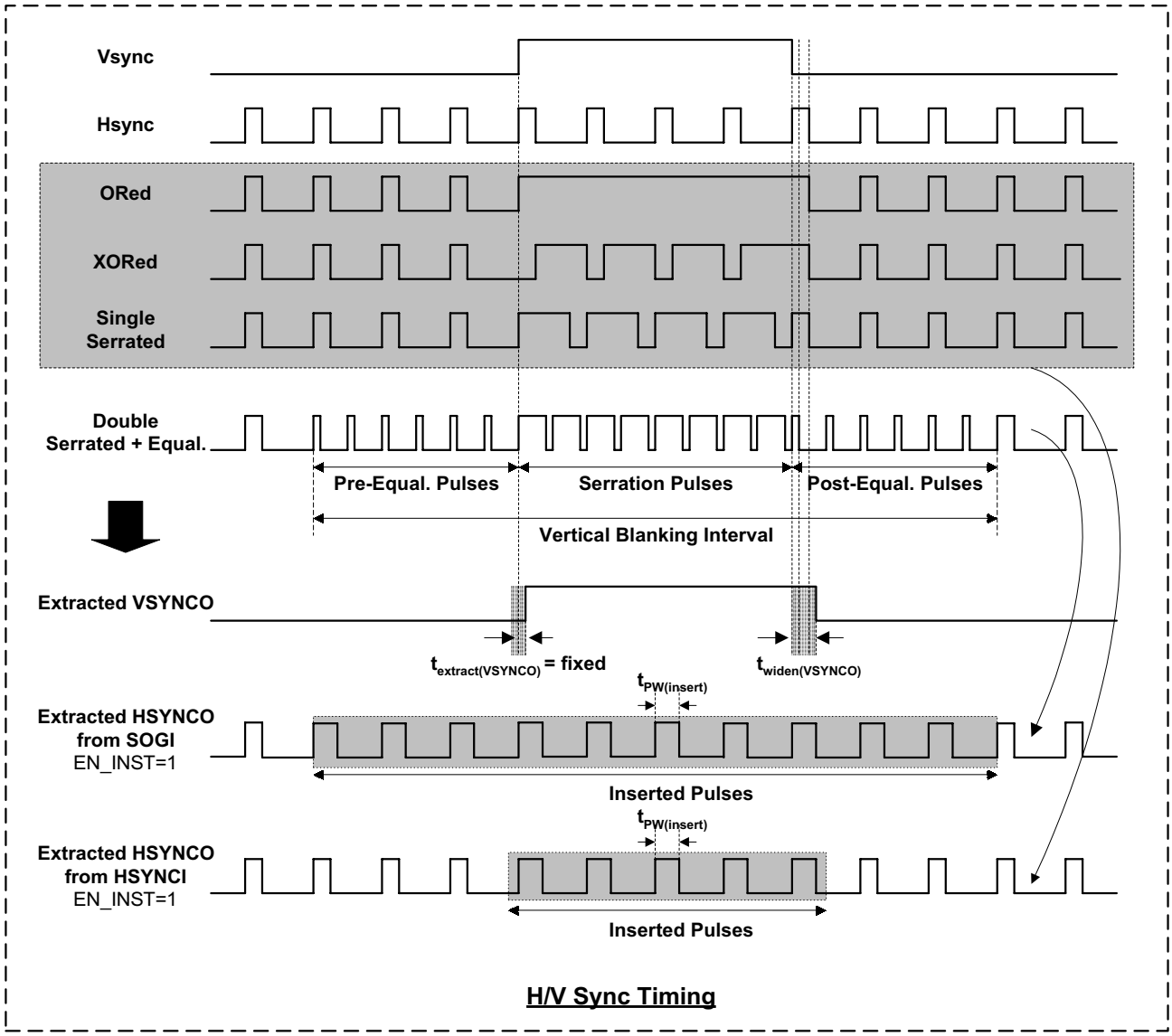
If HGATE=1

2. The Hsync frequency = 12-bit data (HCNT_HB,HCNT_LB)/(Gate Time)

Where Gate Time = 16.384mS when HGATE_TME=0, and Gate Time = 32.768mS when HGATE_TME=1.



8-3 Extract Vsync from Composite/SOG Signal



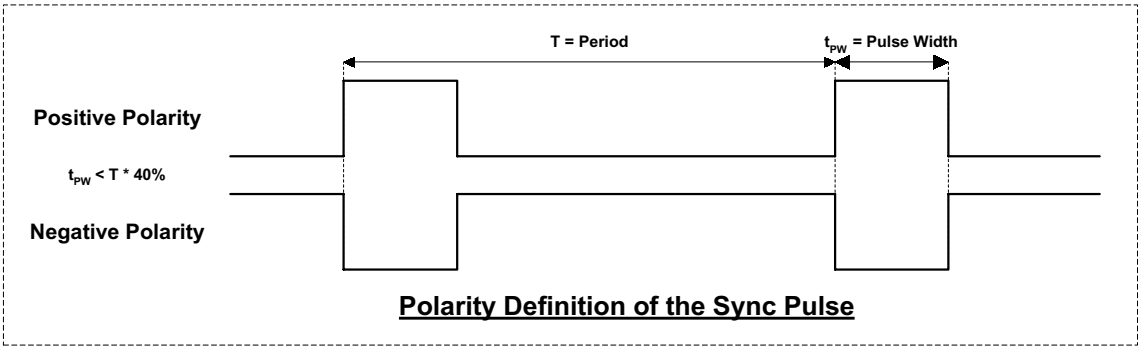
H/V Sync Timing

8-4 Polarity Detection

The sync polarity detection circuit will measure the length of high period of sync and the length of the low period of sync. If the length of the low period is longer than **60%** of the input sync period, the input polarity bit (**HI_POL** or **VI_POL**) will be one, indicating a positive polarity. If the length of the low period is shorter than **40%** input sync period, the input polarity will be zero, negative polarity. The specifications of the polarity detection circuit are listed below.

Spec. Table of H/V Polarity Detect Unit

$f_{VSYNC(SEP)}$	Vsync Frequency from Separate VSYNCI input for Sync Processor	15	-	250	Hz	Vsync Duty Cycle = 40%
f_{VCLK}	Vsync Input Frequency for DDC-1 Mode	-	-	25	KHz	Supply VCLK for DDC-1 mode only
$t_{VPW(SEP)}$	VSYNC input Pulse Width of Separate SYNC	0.150	-	32000	us	Vsync Duty Cycle < 40%
$t_{VPW(COMP)}$	VSYNC input pulse width of Composite/SOG SYNC	0.150	-	2000	us	Vsync Duty Cycle < 40%
f_{HSYNC}	Hsync Input Frequency	15	-	250	KHz	Hsync Duty Cycle = 40%
$t_{HPW(SEP)}$	HSYNC input Pulse Width of Separate-Type SYNC	0.150	-	85	us	Hsync Duty Cycle < 40%
$t_{HPW(COMP)}$	HSYNC input Pulse Width of Composite/SOG SYNC	0.150	-	20.8	us	Hsync Duty Cycle < 40%

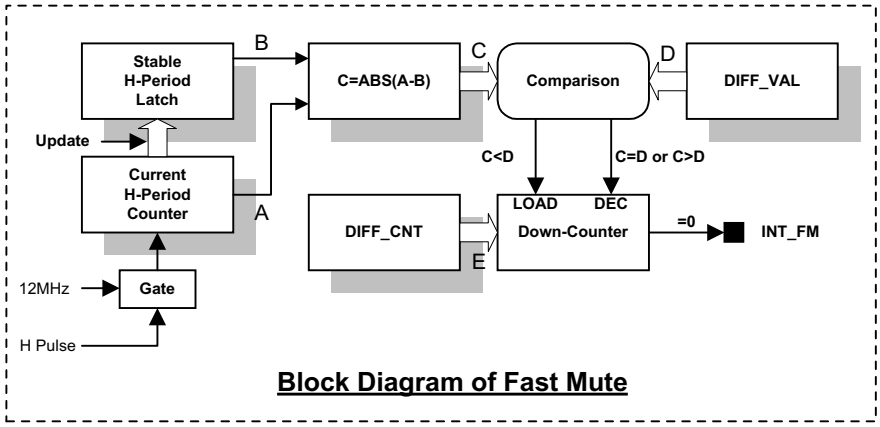


Polarity Definition of the Sync Pulse

8-5 Fast Mute

The block generates a fast mute interrupt, **INT_FM**, to indicate an astable state of horizontal frequency. The operations of this block are:

1. A H-Period Counter counts the 12MHz pulse number within a period of the horizontal sync, and gets the current value **A**
2. The previous stable H-Period Latch held the previous counter value **B**
3. A subtractor gets a difference **C** from **A** and **B**, then B will be replaced with A for updating the next previous value.
4. **C** is compared with the difference bounbary value **DIFF_VAL** written by user.
5. The result C<D loads the content of the **DIFF_CNT**, value **E**, to the Down-Counter to indicate the Hsync input is under a stable condition. It does not affect the flag **INT_FM**.
6. The Down-Counter will decrece its content if the comparison result is C>D or C=D.
7. The flag INT_FM in the INTHV_FLG will be set to 1 if the content of the Down-Counter is decreased to zero, then an **INT_FM** interrupt will be generated when the enable bit **INT_FM** in the register INTHV_EN is enabled.

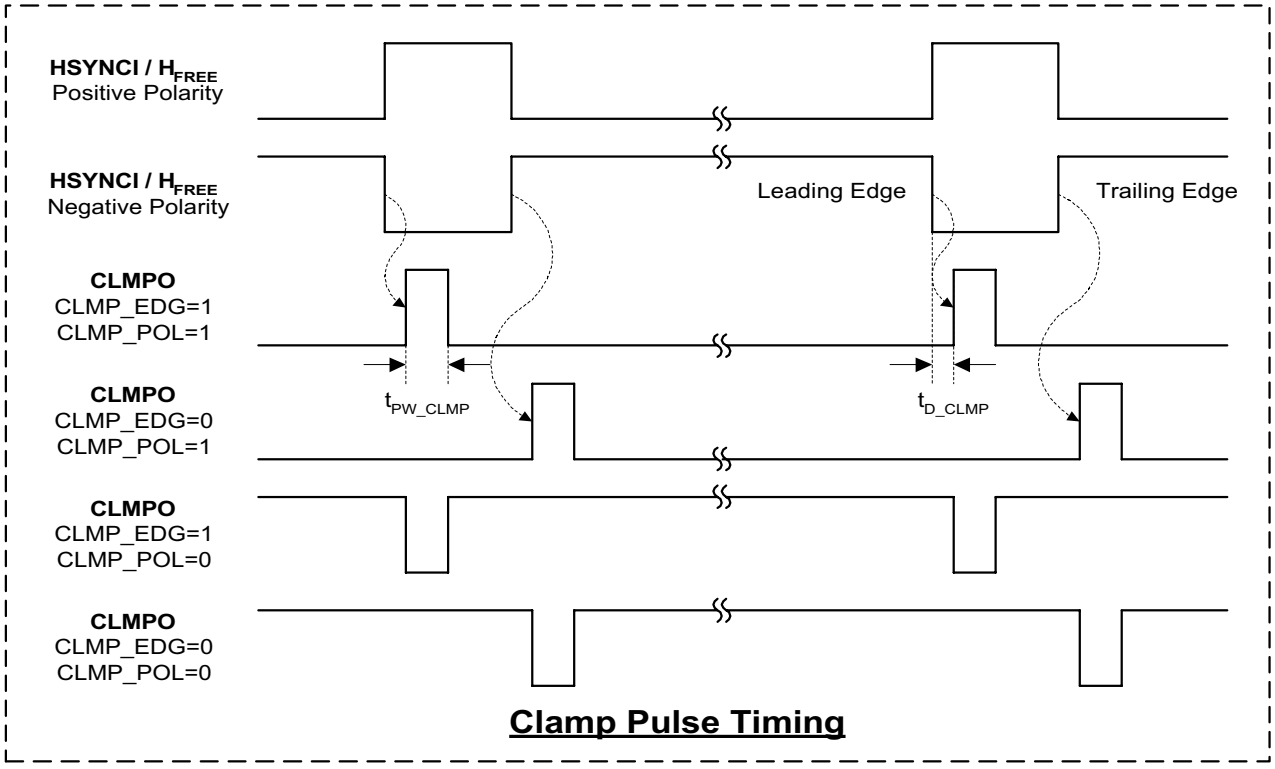


Block Diagram of Fast Mute

8-6 Clamp Pulse Output

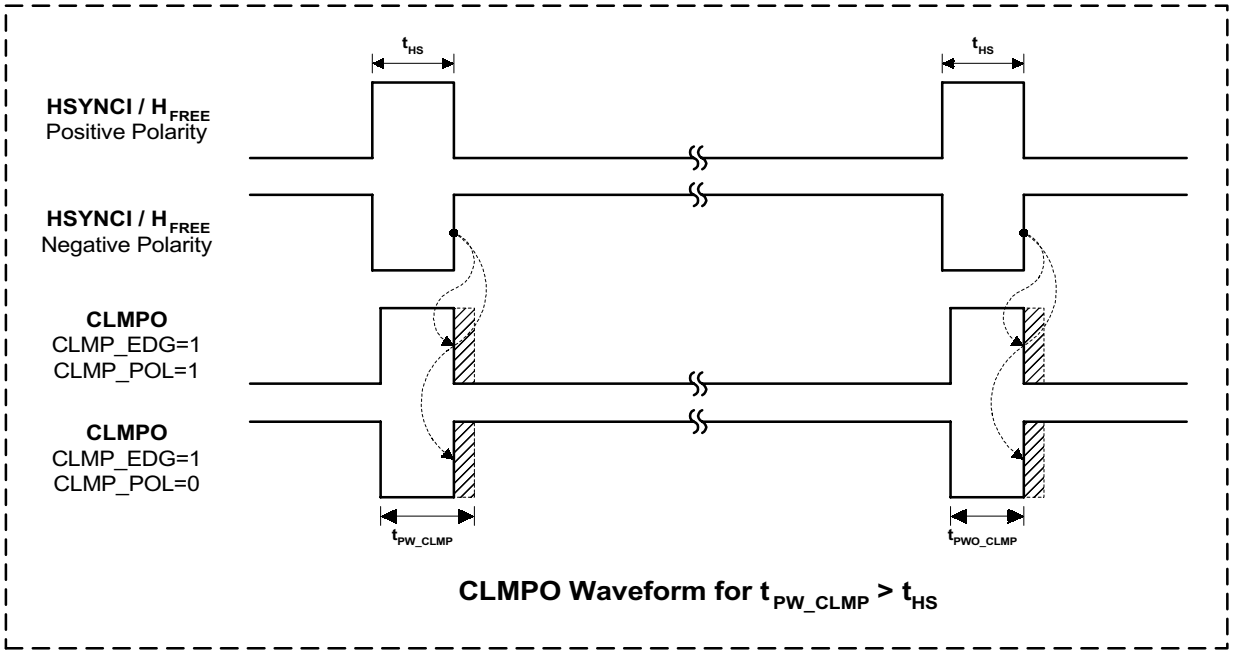
A block circuit called **clamp pulse generator** generates clamp pulse on the **CLMPO** pin, and outputs to the external video Pre-Amplifier for DC restoration. There are two input trigger sources of the clamp generator, one is signal **Hin** from separator and the other is $\mathbf{H_{FREE}}$ from the internal free-run block. If the bit **SYNCO_SEL** is 1 then the Hin input source will be selected, else the H_{FREE} will be selected. The polarity and the trigger egde of the CLMPO can be selected by using bit CLMP_POL and bit CLMP_EDG respectively. The trigger delay of the CLMPO (td_clmp) is less than **50ns**. It is a fixed delay and is independent from the input video timing. The output transient of the CLMPO will not cause any crosstalk and phase jitter. The pulse width of the CLMPO ouput may be selected by bit **CLMP_PW0** and bit **CLMP_PW1**. Refer to the description of the CLMP_REG for details.

➢ ***Clamp Pulse Timing***



Clamp Pulse Timing

CLMPO Output Waveform for t_{PW_CLMP} > t_{HS} under CLMP_EDG=1 condition

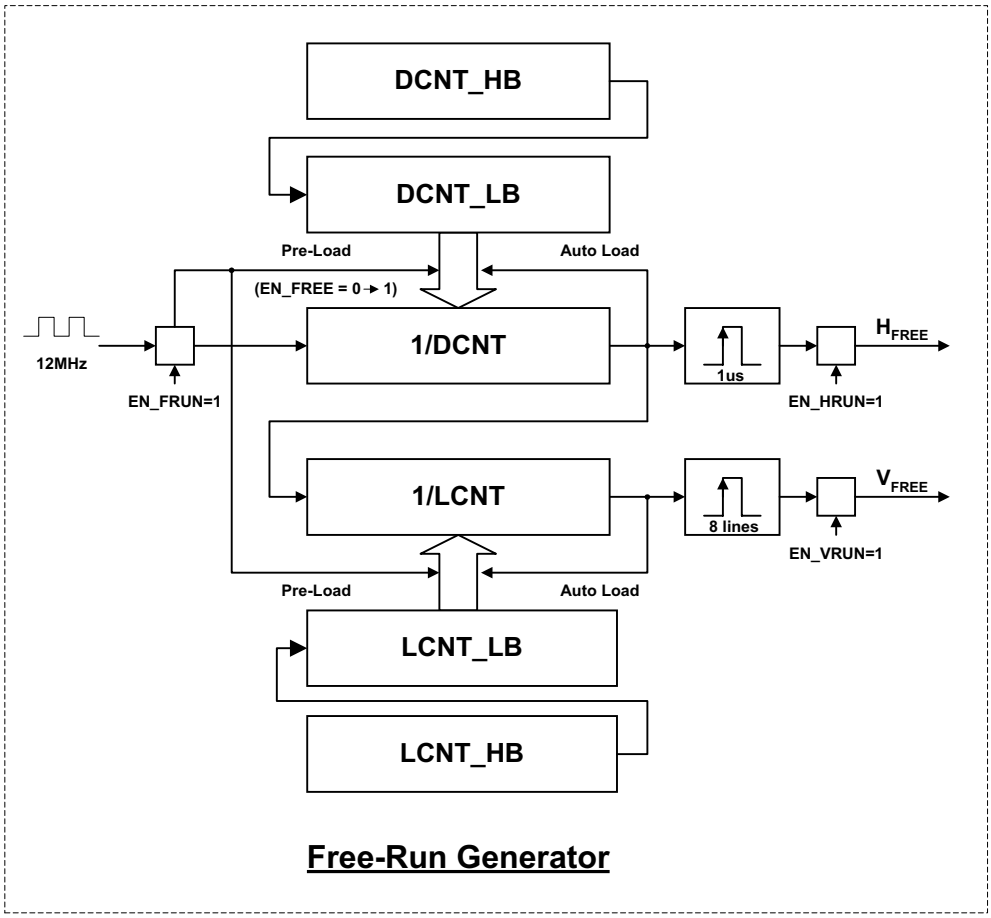


8-7 Free Running

This Block can generate various free-running outputs to satisfy various application requirements. The pulse width of the H_{FREE} output is fixed **1us** and the V_{FREE} is **8 lines**. User can properly set the content of the dot counters, DCNT_HB and DCNT_LB, to get the need frequency of the H_{REEE}, and set the content of the line counters, LCNT_HB and LCNT_LB, to get the frequency of the V_{FREE}. Details refer to the descriptions of the free-run registers DCNT_HB, DCNT_LB, LCNT_HB, and LCNT_LB. Refer to the descriptions of the DCNT register and the LCNT register for details to get user's need frequencies.

The **EN_FRUN** bit can gate the 12MHz clock source to disable this block function and to save power comsuption. The previous values will pre-load into the DCNT/LCNT counters from DCNT_HB, LB / LCNT_HB, LB at the transient of EN_FRUN from 0 to 1. Users also can disable H/V free run output by clearing EN_HRUN / EN_VRUN.

When you want to set the H/V free-running frequency, remember to set the high byte content registers (DCNT_HB, LCNT_HB) first, the H/V frequency will change after you set the low byte contents registers (DCNT_LB, LCNT_LB).

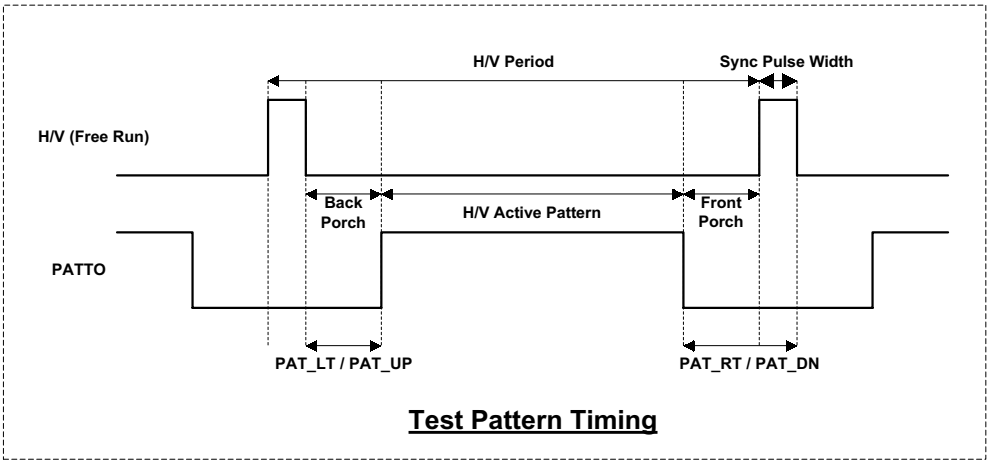


Free-Run Generator

Note：The Pulse width of the H_{FREE} is 1us, and that means it is equally 12 dots under 12MHz OSC.

8-8 Test Pattern

The test pattern generator can generate a **full-white pattern** on the pin PATTO if EN_PAT=1. The content of the PAT_LT is the dot number between the trailing edge of H_{FREE} and the left-side start of the active pattern, and the PAT_RT is the right-side stop. The content of the PAT_UP is the line number between the trailing edge of V_{FREE} and the upper-side start of the active pattern, and the PAT_DN is the lower-side stop. User can properly set the parameters to output a proper test pattern after setting the parameters of the free-run generator.



Test Pattern Timing

- The pulse width of the H_{FREE} is 12 dots and the pulse width of the V_{FREE} is 8 lines, so
  - ❶ Front Porch of H_{FREE} = (PAT_RT) – 12,
  - ❷ Back Porch of H_{FREE} = (PAT_LT),
  - ❸ Front Porch of V_{FREE} = (PAT_DN) – 8, and
  - ❹ Back Porch of V_{FREE} = (PAT_UP)
- The min. value of the PAT_RT content is 12 for test pattern generator, and PAT_DN is 8. There is any test-pattern within Sync pulse intervals of H_{FREE} and of V_{FREE}

Register	PAT_LT	Left-Side Dot Number of the Test Pattern Output	
B7	X	-	Unused
B6 ~ B0	PAT_LT6 ~ PAT_LT0	W	Dot number between the trailing edge of H_{FREE} and the left-side start of the active pattern. ☑Dot frequency = f_{OSC}

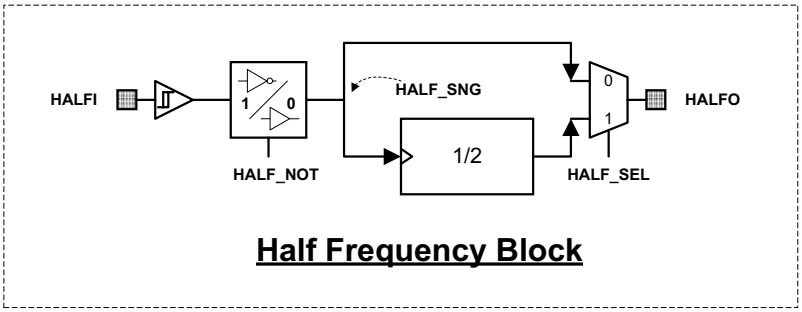
Register	PAT_RT	Right-Side Dot Number of the Test Pattern Output	
B7	X	-	Unused
B6 ~ B0	PAT_RT6 ~ PAT_RT0	W	Dot number between the trailing edge of H_{FREE} and the right-side stop of the active pattern. ☑Dot frequency = f_{OSC}

Register	PAT_UP	Upper-Side Line Number of the Test Pattern Output	
B7 ~ B0	PAT_UP7 ~ PAT_UP0	W	Line number between the trailing edge of V_{FREE} and the upper-side start of the active pattern.

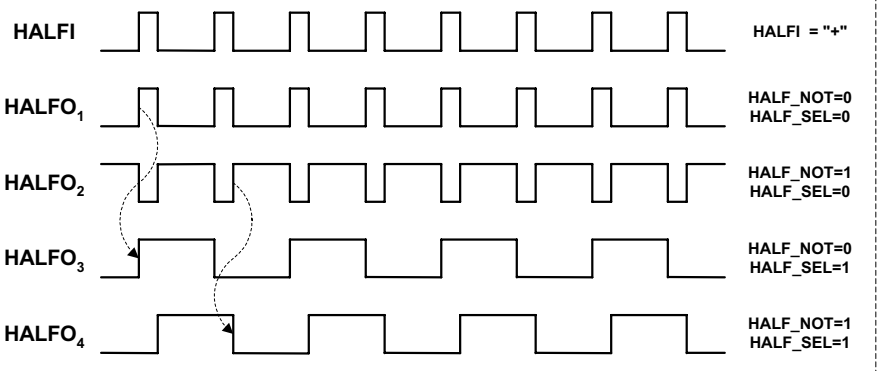
Register	PAT_DN	Lower-Side Line Number of the Test Pattern Output	
B7 ~ B0	PAT_DN7 ~ PAT_DN0	W	Line number between the trailing edge of V_{FREE} and the lower-side stop of the active pattern.

8-9 Half Frequency Input/Output

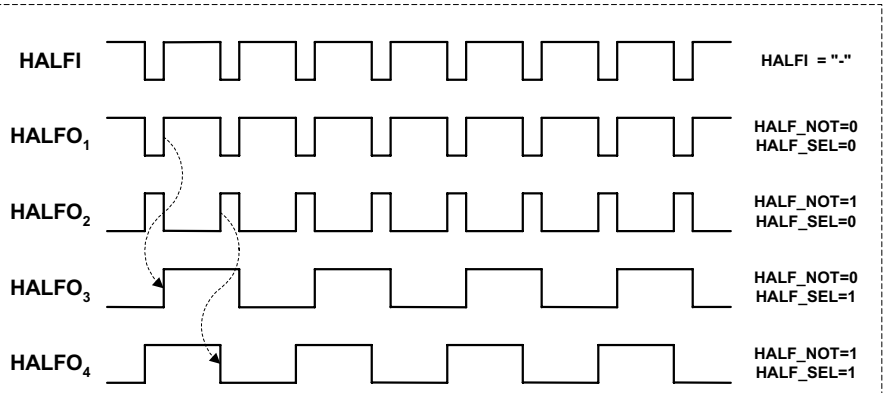
The HALFO Output is a half frequency square waveform of the HALFI input if the HALF_SEL bit is 1 under **EN_HALF=1** condition, else the HALFO will be as the same as the HALFI input. This function supplies a half frequency output to apply. User also can properly control the output polarity of the HALFO by setting the HALF_NOT bit. The detail block and timings are as shown as follows.



Half Frequency Block



HALFO Timing (HALFI Polarity = "+")



HALFO Timing (HALFI Polarity = "-")

Registers

Register	INTHV_FLG	H/V Interrupt-Flag Register	
B7	INT_H	R	1: Hsync leading edge interrupt from separate or composited signal 0: no interrupt
B6	INT_V	R	1: Vsync leading edge interrupt from separate or composited signal 0: no interrupt
B5	X	-	Unused
B4	X	-	Unused
B3	X	-	Unused
B2	INT_HP	R	H-Polarity Change INT 1:Input Polarity of Hsync changes. 0:unchange
B1	INT_VP	R	V-Polarity Change INT 1: It will be activated when the Input Polarity of Vsync changes. 0:unchange
B0	INT_FM	R	Fast Mute INT 1:Fast Mute Interrupt is activated. 0:Fast Mute does not appear

Register	INTHV_CLR	H/V Interrupt-Flag Register	
B7	INT_H	W	1:Clear it 0: No effect
B6	INT_V	W	1:Clear it 0: No effect
B5	X	-	Unused
B4	X	-	Unused
B3	X	-	Unused
B2	INT_HP	W	1:Clear it 0: No effect
B1	INT_VP	W	1:Clear it 0: No effect
B0	INT_FM	W	1:Clear it 0: No effect

Register	INTHV_EN	H/V interrupt-Enable Register	
B7	INT_H	W	1:Enable 0: Disable
B6	INT_V	W	1:Enable 0: Disable
B5	X	-	Unused
B4	X	-	Unused
B3	X	-	Unused
B2	INT_HP	W	1:Enable 0: Disable
B1	INT_VP	W	1:Enable 0: Disable
B0	INT_FM	W	1:Enable 0: Disable

Register	SYNC_REG	Sync Processor Control register	
B7	EN_FRUN	W R	1:Enable Free-Run function. 0:Disable Free-Run function to save power consumption.
B6	AUTO_FLT	W R	1:Enable Auto Filter function of H/V Extract Circuit. 0:Disable Auto-Filter function
B5	EN_SOG	W R	SOG function Control Bit 1:Enable SOG function 0:Disable SOG function
B4	EN_CLMP	W R	Enable Clamp output 1:Enable Clamp function 0:Disable Clamp function
B3	EN_PATT	W R	Control Bit of the Pattern Generator Output 1:Enable the PATTern function ☑Test pattern may output on the PATTO pin if the SYNCO_SEL=1(Free Running) 0:Disable the PATTern function
B2	EN_HALF	W R	HALF function Enable Bit 1:Enable HALF function; HALFI and HALFO are the I/O pin assignment. 0:Disable HALF function
B1	HALF_SEL	W R	HALFO output frequency selection (see “HALF Frequency Block” diagram) 1:HALFO is a half frequency of HALF_SNG square waveform 0:HALFO is the same as HALF_SNG
B0	HALF_NOT	W R	HALFO output Polarity/Edge selection 1:HALF_SNG : Invert HALFI 0:HALF_SNG : Bypass HALFI

Register	HVO_REG	HSYNCO/VSYNCO Control Register	
B7	EN_HOUT	W R	1:Enable HSYNCO Output Pin 0:Disable HSYNCO Output
B6	EN_VOUT	W R	1:Enable VSYNCO Output 0:Disable VSYNCO Output
B5	EN_HRUN	W R	Free-run Horizontal output Control 1:Enable 0:Disable
B4	EN_VRUN	W R	Free-run Vertical output Control 1:Enable 0:Disable
B3	EN_INS	W R	Insert pulse Control 1:Enable 0:Disable
B2	SYNCO_SEL	W R	Source Selection Control of Sync outputs(HSYNCO and VSYNCO) 1:Sync outputs from the internal free running generator(H_{FREE} and V_{FREE}) 0:Sync outputs from the external sync inputs(H_{in} and V_{in})
B1	HO_POL	W R	Horizontal Output Polarity Selection 1:Positive polarity 0:Negative polarity ☑Free-Running also must be under control
B0	VO_POL	W R	Vertical Output Polarity Selection 1:Positive polarity 0:Negative polarity ☑Free-Running also must be under control

Register	HVI_REG	H-/V-Sync Input Control Register	
B7	SYNCI_SEL1	W R	Type Selection of Sync Input: 0X:Composite Sync from SOGI
B6	SYNCI_SEL0	W R	10:Composite Sync from HSYNCI 11:Separate Sync from HSYNCI /VSYNCI
B5	INS_PW	W R	Pulse Width Selection of Insert Pulse 0:Insert Pulse width ➨ The content of **HPW_REG** counted from HSYNCI/SOGI. 1:Insert Pulse width ➨ Fixed 1us pulse width.
B4	X	-	Unused
B3	HS_LVL	R	The Input Digital Level of HSYNCI Pin at this sampling moment 0:Low Level 1:High Level
B2	VS_LVL	R	The Input Digital Level of VSYNCI Pin at this sampling moment 0:Low Level 1:High Level
B1	HI_POL	R	H-Polarity Flag Detected by Input Polarity Detection Circuit 0:Negative polarity ☑the high period is longer than **60%** of input sync period 1:Positive polarity ☑the low period is longer than **60%** of input sync period
B0	VI_POL	R	V-Polarity Flag Detected by Input Polarity Detection Circuit 0:Negative polarity ☑the high period is longer than **60%** of input sync period 1:Positive polarity ☑the low period is longer than **60%** of input sync period

Register	HPW_REG	H-Pulse Width Register	
B7~B0	HPW7 ~ HPW0	R	Pulse Width of the External HSYNCI Input. Unit : 83.3ns/count ☑ Clock Source = 12MHz OSC

Register	HFLT_REG	Hsync Filter Register	
B7~B0	HFLT7 ~ HFLT0	W R	Time Width of Pulse Filter for Composite Sync Extraction Unit : 83.3ns/count ☑ Clock Source = 12MHz OSC

Register	CLMP_REG	Clamp pulse Control Register	
B7	X		Unused
B6	X		
B5	X		
B4	X		
B3	CLMP_EDG	W	Trigger Edge of the Clamp Pulse 0: Clamp pulse is at the trailing edge of H_{IN}/H_{FREE} 1:Clamp pulse is at the leading edge of H_{IN}/H_{FREE}
B2	CLMP_POL	W	Clamp-Pulse Output Polarity Selection 0:Negative polarity 1:Positive polarity
B1	CLMP_PW1	W	Clamp Pulse Width Selection 00 ➨ 0.25us 01 ➨ 0.5us 10 ➨ 1us 11 ➨ 2us
B0	CLMP_PW0	W	

Register	PAT_LT	Left-Side Dot Number of the Test Pattern Output	
B7	X	-	Unused
B6 ~ B0	PAT_LT6 ~ PAT_LT0	W	Dot number between the trailing edge of H_{FREE} and the left-side start of the active pattern. Dot frequency = f_{OSC}

Register	PAT_RT	Right-Side Dot Number of the Test Pattern Output	
B7	X	-	Unused
B6 ~ B0	PAT_RT6 ~ PAT_RT0	W	Dot number between the trailing edge of H_{FREE} and the right-side stop of the active pattern. Dot frequency = f_{OSC}

Register	PAT_UP	Upper-Side Line Number of the Test Pattern Output	
B7 ~ B0	PAT_UP6 ~ PAT_UP0	W	Line number between the trailing edge of V_{FREE} and the upper-side start of the active pattern.

Register	PAT_DN	Lower-Side Line Number of the Test Pattern Output	
B7 ~ B0	PAT_DN6 ~ PAT_DN0	W	Line number between the trailing edge of V_{FREE} and the lower-side stop of the active pattern.

Register	HVCNT_CTRL	Control Register for Hsync/Vsync Counter	
B7	X	-	Unused
B6	X	-	Unused
B5	X	-	Unused
B4	X	-	Unused
B3	VOV_SEL1	W	**Overflow Time interval Control Bits of Vsync Counter** 00 ➡ 32.768ms 01 ➡ 65.536ms 10 ➡ 98.304ms 11 ➡ 131.072ms
B2	VOV_SEL0	W	
B1	HGATE_SRC	W	Gate Source control bit for Hsync Counter 0 ➡ From Vsync Period 1 ➡ Fom Internal Time Gate;see HGATE_TME bit in this byte
B0	HGATE_TME	W	**Gate Time control bit for Hsync Counter** 0 ➡ 16.384ms 1 ➡ 32.768ms

Register	HCNT_HB	High-Byte Content of the Hsync Counter	
B7	HCNTOV	R	Overflow Flag of Hsync Counter 1:Overflow 0:Normal
B6	X	-	Unused
B5	X	-	Unused
B4	X	-	Unused
B3 ~ B0	HCNT11 ~ HCNT8	R	High-Byte Content of the H-Counter

Register	HCNT_LB	Low-Byte Content of the Hsync Counter	
B7 ~ B0	HCNT7 ~ HCNT0	R	Low-Byte Content of the H-Counter

Register	VCNT_HB	High-Byte Content of the Vsync Counter	
B7	VCNTOV	R	Overflow Flag of Vsync Counter 1:Overflow 0:Normal
B6	X	-	Unused
B5 ~ B0	VCNT13 ~ VCNT8	R	Low-Byte Content of the V-Counter

Register	VCNT_LB	Low-Byte Content of the Vsync Counter	
B7 ~ B0	VCNT7 ~ VCNT0	R	Low-Byte Content of the V-Counter

Register	DCNT_HB	High Byte Content of Dot Divider in Free Running Block	
B7	X	-	Unused
B6	X	-	
B5	X	-	
B4	X	-	
B3	X	-	
B2	X	-	
B1	X	-	
B0	DCNT8	W	High order Bit 8 of the Dot Divider Content for Horizontal Free Running: See the DCNT_LB Register Description, please.

Register	DCNT_LB	Low Byte Content of Dot Divider in Free Running Block	
B7	DCNT7	W	**Written Content of Dot Divider for Horizontal free running**: ①Bit Number = 9 Bits ②Dot Clock = 12MHz ③Valid Range = 48 ~ 511 If out of this valid range, the reset default values will be loaded into DCNT & LCNT to protect the following circuit. ④Horizontal Frequency of the free running is **Hfreq(free) = 12MHz / DCNT** (ex) if 100KHz free-run horizontal frequency is wanted, then the following divider content will be set DCNT = 12MHz / 100KHz =120(dec) = 78(hex) ⑤**Hfreq** will change after you write this byte
B6	DCNT6	W	
B5	DCNT5	W	
B4	DCNT4	W	
B3	DCNT3	W	
B2	DCNT2	W	
B1	DCNT1	W	
B0	DCNT0	W	

Register	LCNT_HB	High Byte Content of Line Divider in Free Running Block	
B7	X	-	Unused
B6	X	-	
B5	X	-	
B4	X	-	
B3	X	-	
B2	LCNT10	W	High order Bit 8 ~ Bit 10 of the line Divider Content for Vertical Free Running: See the LCNT_LB Register Description, please.
B1	LCNT9	W	
B0	LCNT8	W	

Register	LCNT_LB	Low Byte Content of Line Divider in Free Running Block	
B7	LCNT7	W	**Written Content of Line Divider for Vertical free running**: ①Bit Number = 11 Bits ②Line Clock = Hfreq(free) ③Valid Range = 100 ~ 2047 if out of this valid range, the reset default values will be loaded into DCNT & LCNT to protect the following circuit. ④Vertical Frequency of the free running is **Vfreq(free) = Hfreq(free)/LCNT = (12MHz / DCNT) / LCNT** (ex) if 100Hz free-run vertical frequency is wanted at Hfreq(free)=100KHz condition, then the following Line divider content will be set LCNT = 100KHz / 100Hz =1000(dec) = 3E8(hex) ⑤**Vfreq** will change after you write this byte
B6	LCNT6	W	
B5	LCNT5	W	
B4	LCNT4	W	
B3	LCNT3	W	
B2	LCNT2	W	
B1	LCNT1	W	
B0	LCNT0	W	

Register	MUTE_CTRL	Mute Control Register	
B7	UPD_HT	W R	0: Hold B 1: Updated B from A, see Fast Mute Block Diagram. ☑ This bit is Controlled by S/W if AUTO_UPD=0.
B6	AUTO_UPD	W R	0: Manually Control the UPD_HT bit 1: H/W automatically sets UPD_HT to update B from A when the fast mute occurs, then it cleares UPD_HT after the input Hsync has been stable at least 3ms.
B5	HS_ACT	R	0: No Hsync in 3ms interval 1: Hsync is active
B4	VS_ACT	R	0: No Vsync in 132ms interval 1: Vsync is active
B3 ~ B2	DIFF_CNT1 ~ DIFF_CNT0	W R	The FAST MUTE will occur if the times out of DIFF_VAL are more than DIFF_CNT setting 00 ➨ 4 times 01 ➨ 8 times 10 ➨ 16 times
B1 ~ B0	DIFF_VAL1 ~ DIFF_VAL0	W R	Difference Boundary of the H-Period Counter 00 ➨ 4 counts 01 ➨ 8 counts 10 ➨ 16 counts

Section-9 A/D Converters

The ADC is a 7-bit 4-channel analog-to-digital converter. The structure of these ADCs is 7-bit successive approximation. Analog voltage is supplied from external sources to the A/D input pins and the result of the conversion is stored in the 7-bit data latch registers (**ADC0_REG ~ ADC3_REG**). The A/D channels are activated by clearing the correspondent control bits in the ADC_CON control register. When users write '1' into one of the enable control bits (**EN_ADC0 ~ EN_ADC3**), its correspondent I/O pin will be switched to the A/D converter input pin.

The conversion will be started by setting **STRT_ADC** bit (CONVERSION START) in the ADC_CON control register. When conversion is finished, the system will set this **CMPL_ADC** bit. Users can monitor this bit to get the valid A/D conversion data in the A/D latch registers (**ADC0_REG ~ ADC3_REG**). Note that only at the activated A/D channel, its latched data is meaningful. The analog voltage to be measured should be stabled during the conversion operation and the variation will not exceed 1 LSB for the best precision in measurement.

Conversion Time

- Less than 12us for 4 ADC channels totally.
- It converts these 4-channel inputs to digital values and stores them into the ADCx_REG channel by channel sequentially.

Conversion Range: GND to VCC

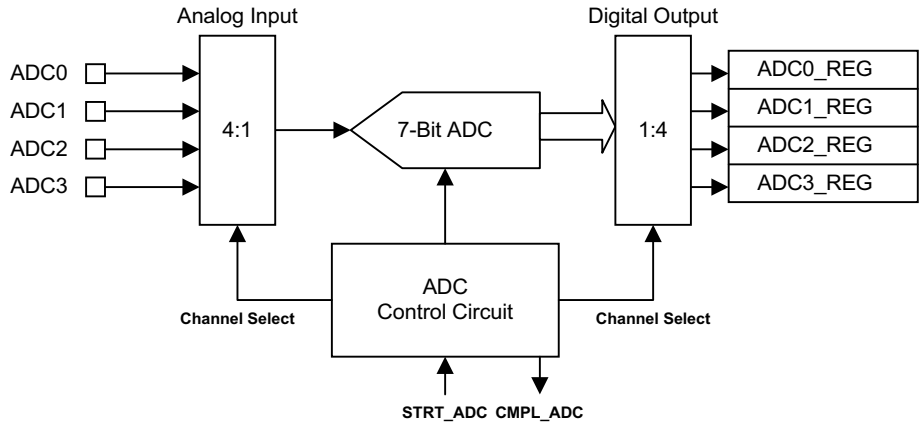
- If the input voltage is GND or less than GND, the ADC conversion result will be $00.
- If the input voltage is VCC or large than VCC, the ADC conversion will be $7F.
- If the input voltage is between GND and VCC, the ADC wil be a linear conversion result.

Conversion Precision and Accuracy:

- Linear conversion
- Absolutely monotonic
- No missing codes

Conversion Result:

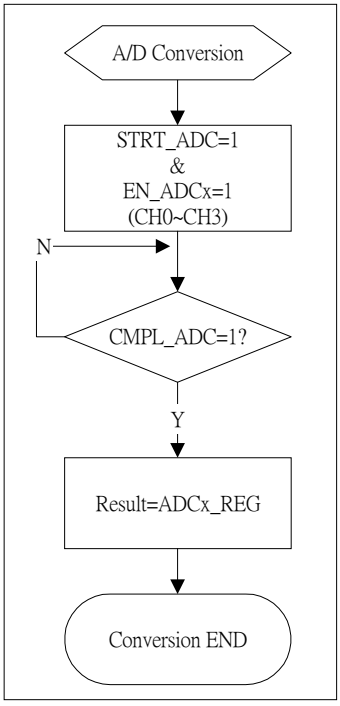
$$\frac{V_{CC}}{(2^7-1)} \times ADC\_REG = ADC\_IN(DEC)$$



A/D Converter Block Diagram

Users can enable ADCs (EN_ADCx=1) and start ADC (STRT_ADC=1) simultaneously in an instruction.

Flow Chart of the A/D Converter



Note:
1. You can select ADC channel and start conversion simultaneously.
2. The ADC conversion result register is invalid if you do not enable this channel.
3. The conversion time is independent of the number of channels you select.

Registers:

Register	ADC_CON	A/D Converter Control Register	
B7	STRT_ADC	W	Control Signal to Start the A/D Convert 1:Start the A/D Conversion. CMPL_ADC will be clear after writing 1 to this bit. 0: No Effect
B6	X	—	Unused
B5	X	—	Unused
B4	X	—	Unused
B3	EN_ADC3	R/W	Enable Bit for A/D Converter 3 1:Enable 0:Disable ADC3; and this pin will be assigned as GPIO pin
B2	EN_ADC2	R/W	Enable Bit for A/D Converter 2 1:Enable 0:Disable ADC2; and this pin will be assigned as GPIO pin
B1	EN_ADC1	R/W	Enable Bit for A/D Converter 1 1:Enable 0:Disable ADC1; and this pin will be assigned as GPIO pin
B0	EN_ADC0	R/W	Enable Bit for A/D Converter 0 1:Enable 0:Disable ADC0; and this pin will be assigned as GPIO pin

Register	ADC0_REG	Conversion Data Register of ADC Channel 0	
B7	X	—	Unused
B6 - B0	ADC06 - ADC00	R	Converted digital content of the A/D Converter 0

Register	ADC1_REG	Conversion Data Register of ADC Channel 1	
B7	X	—	Unused
B6 - B0	ADC16 - ADC10	R	Converted digital content of the A/D Converter 1

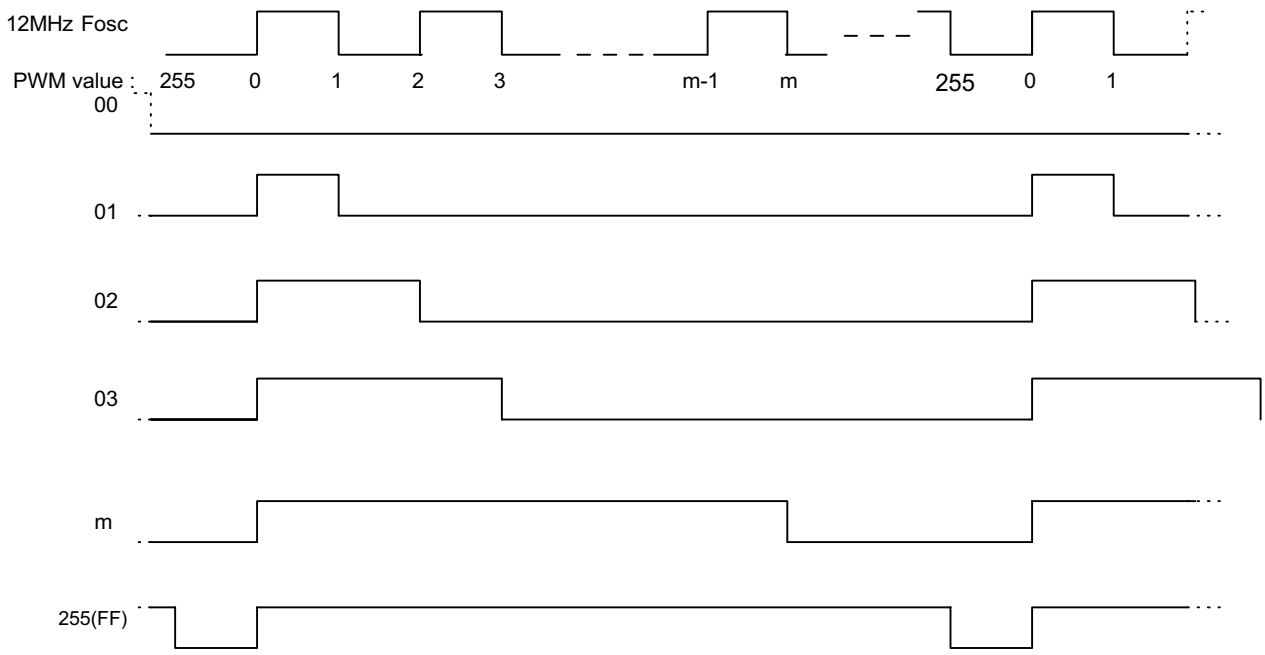
Register	ADC2_REG	Conversion Data Register of ADC Channel 2	
B7	X	—	Unused
B6 - B0	ADC26 - DC20	R	Converted digital content of the A/D Converter 2

Register	ADC3_REG	Conversion Data Register of ADC Channel 3	
B7	CMPL_ADC	R	Conversions Complete Flag 1:A/D Conversion has been completed 0:A/D Conversion does not be completed yet
B6 - B0	ADC36 - ADC30	R	Converted digital content of the A/D Converter 3

Section-10 PWM D/A Converters

There are 10 PWM D/A converters with 8-bit resolution. Almost all D/A converters are Push-Pull output structure with external 3.3V applied maximum except the PWM6~PWM9. All the PWM DAC outputs (PWM0 – PWM9) are shared with I/O pins. Those shared PWM channels are activated by setting the correspondent control bits in the **ENPWM_HB and ENPWM_LB** control registers. When users write '1' into one of the enable control bits, its correspondent I/O pin will be switched to PWM output pin. Please refer to the **Section7 I/O Ports** for the detailed pin configuation.

The PWM refresh rate is 93.75KHz operating on 12MHz system clock. There are 10 readable PWMx_REG registers corresponding to 10 PWM DAC output channels. Each PWM output pulse width is programmable by setting the 8-bit digital to the corresponding PWM_REGx registers. When these PWM_REGx registers are set to 00H, the PWM DAC will output LOW (GND level) and every 1-bit addition will add 41.67 ns pulse width. After reset, all DAC outputs are set to 80H. (Please refer to the following figure for the detailed timing diagram of PWM D/A output.)



PWM DAC Output Timing Diagram and Wave Table

Registers:

Register	ENPWM_HB	High Byte of PWM Enable Register for PWM2 ~ PWM9	
B7	EN_PWM9	R/W	1:Enable PWM9 0:Disable PWM9
B6	EN_PWM8	R/W	1:Enable PWM8 0:Disable PWM8
B5	EN_PWM7	R/W	1:Enable PWM7 0:Disable PWM7
B4	EN_PWM6	R/W	1:Enable PWM6 0:Disable PWM6
B3	EN_PWM5	R/W	1:Enable PWM5 0:Disable PWM5
B2	EN_PWM4	R/W	1:Enable PWM4 0:Disable PWM4
B1	EN_PWM3	R/W	1:Enable PWM3 0:DisablePWM 3
B0	EN_PWM2	R/W	1:Enable PWM2 0:Disable PWM2

Register	ENPWM_LB	Lower Byte of PWM Enable Register for PWM0 ~ PWM1	
B7	X	—	Unused
B6	X	—	Unused
B5	X	—	Unused
B4	X	—	Unused
B3	X	—	Unused
B2	X	—	Unused
B1	EN_PWM1	R/W	1:Enable PWM1 0:DisablePWM 1
B0	EN_PWM0	R/W	1:Enable PWM0 0:DisablePWM 0

Register	PWM0_REG	PWM0 Content Register	
B7 - B0	PWM0_7 - PWM0_0	W R	PWM Content of Channel 0 $80:default Value

Register	PWM1_REG	PWM1 Content Register	
B7 - B0	PWM1_7 - PWM1_0	W R	PWM Content of Channel 1 $80:default Value

Register	PWM2_REG	PWM2 Content Register	
B7 - B0	PWM2_7 – PWM2_0	W R	PWM Content of Channel 2 $80:default Value

Register	PWM3_REG	PWM3 Content Register	
B7 - B0	PWM3_7 – PWM3_0	W R	PWM Content of Channel 3 $80:default Value

Register	PWM4_REG	PWM4 Content Register	
B7 - B0	PWM4_7 – PWM4_0	W R	PWM Content of Channel 4 $80:default Value

Register	PWM5_REG	PWM5 Content Register	
B7 - B0	PWM5_7 – PWM5_0	W R	PWM Content of Channel 5 $80:default Value

Register	PWM6_REG	PWM6 Content Register	
B7 - B0	PWM6_7 – PWM6_0	W R	PWM Content of Channel 6 $80:default Value

Register	PWM7_REG	PWM7 Content Register	
B7 - B0	PWM7_7 – PWM7_0	W R	PWM Content of Channel 7 $80:default Value

Register	PWM8_REG	PWM8 Content Register	
B7 - B0	PWM8_7 - PWM8_0	W R	PWM Content of Channel 8 $80:default Value

Register	PWM9_REG	PWM9 Content Register	
B7 - B0	PWM9_7 - PWM9_0	W R	PWM Content of Channel 9 $80:default Value

Section-11 Multi-Master I²C-Bus

11-1 General Description

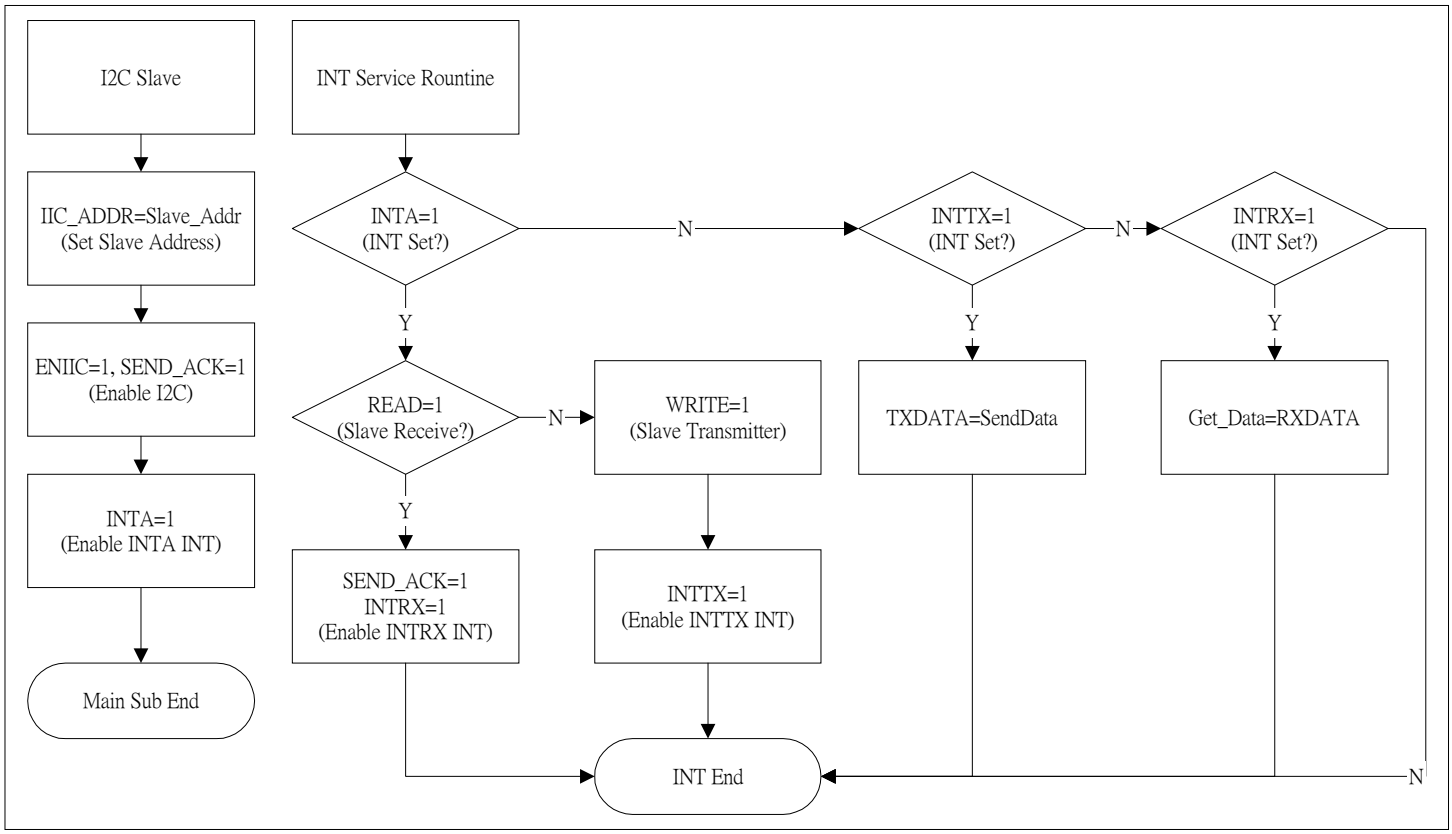
We have a built-in I²C bus which support multi-master and have the folling features:

- Slave mode
- Multi-master mode
- Compatible with the I²C bus specification
- Adjustable I²C slave address (**IIC_ADDR**)
- Automatic hardware wait state generation
- Interrupt control of the I²C bus status control
- Detection of the “START” and “STOP” condition on the I²C bus
- Force to generate “START” and “STOP” command on the I²C bus (**START_GEN**, **STOP_GEN**)
- Two level FIFO to make the protocol more efficent
- Support up to 400Kbps in master mode
- Hardware clock synchronization
- Interrupt generation of the arbitration lose

You can enable the I²C function by setting the control bit **ENIIC=1**. After you enable the I²C the system is staying in slave mode and waiting for the master to address it.

11-2 Slave Mode of the I²C Bus

Flow Chart of I²C Slave



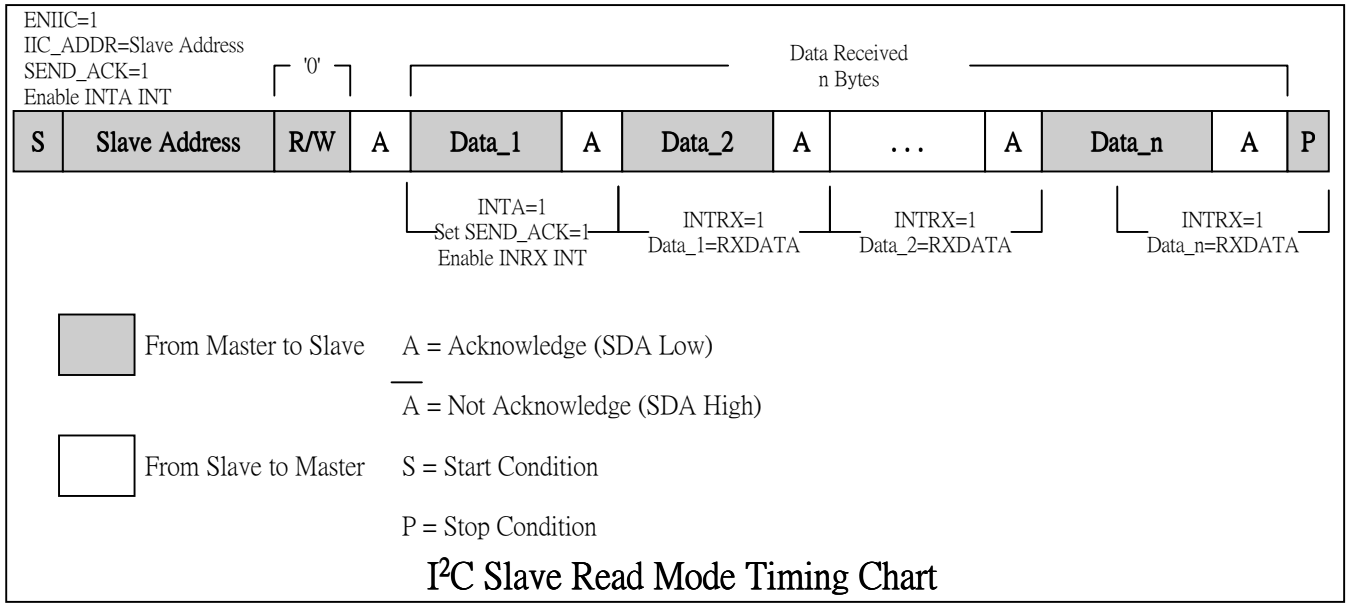
Note:

1. In our design, we reserve two level shift registers for transmission and reception. So you can try to read/write two byte data in the same time if the second level TX/RX buffer is empty/full (***TX_NULL=1*** or ***RX_FULL=1***).

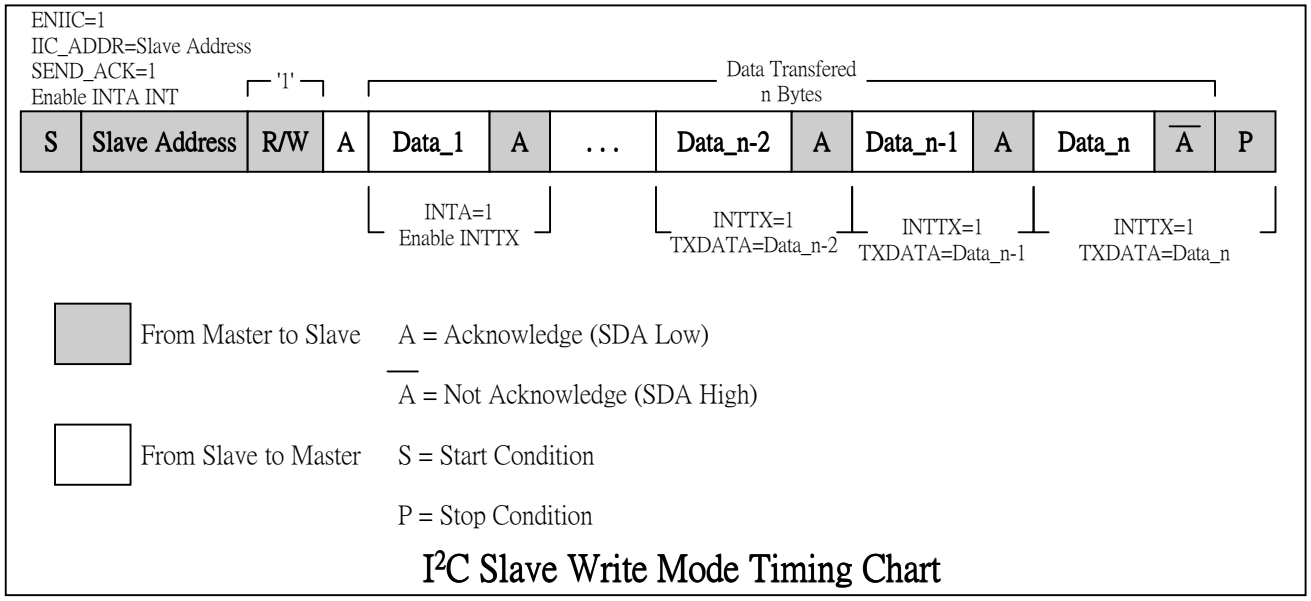
2. During the I²C transmission interval (RX/TX) if you want to generate a "WAIT" state manually, you can set the control register ***WAIT=1*** and force to pull the SCL low until you release the bus line (***WAIT=0***).

3. In receiver mode, after the ***INTRX=1*** if you want discard this data, you can set the ***CLR_FIFO=1*** to force empty the receive buffer without interrupt.

4. If you want to clear the transmission buffer, you can set the ***CLR_TX_FIFO=1*** to force to empty the transmission buffer.



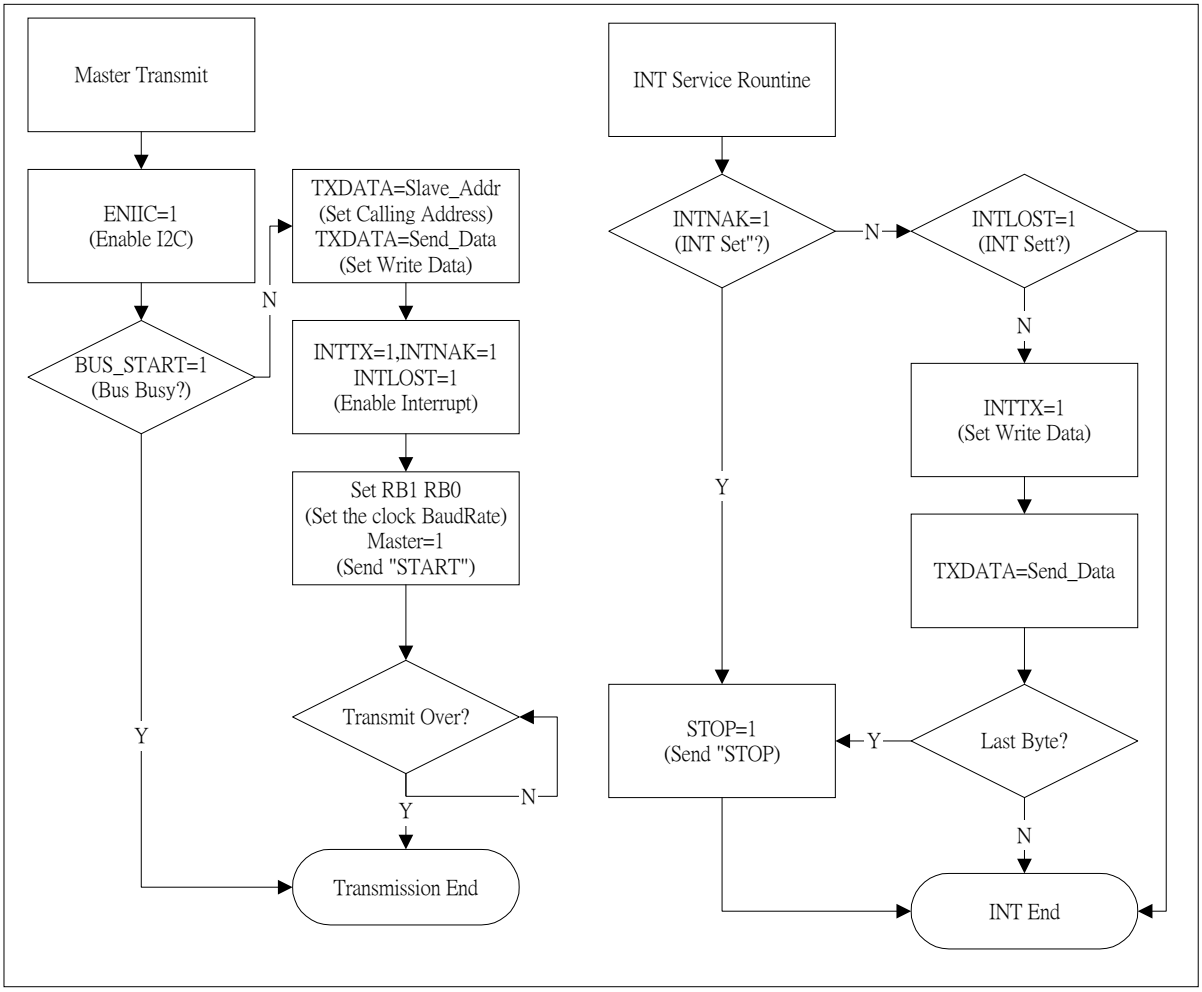
I²C Slave Read Mode Timing Chart



I²C Slave Write Mode Timing Chart

11-3 Master Mode of the I²C Bus

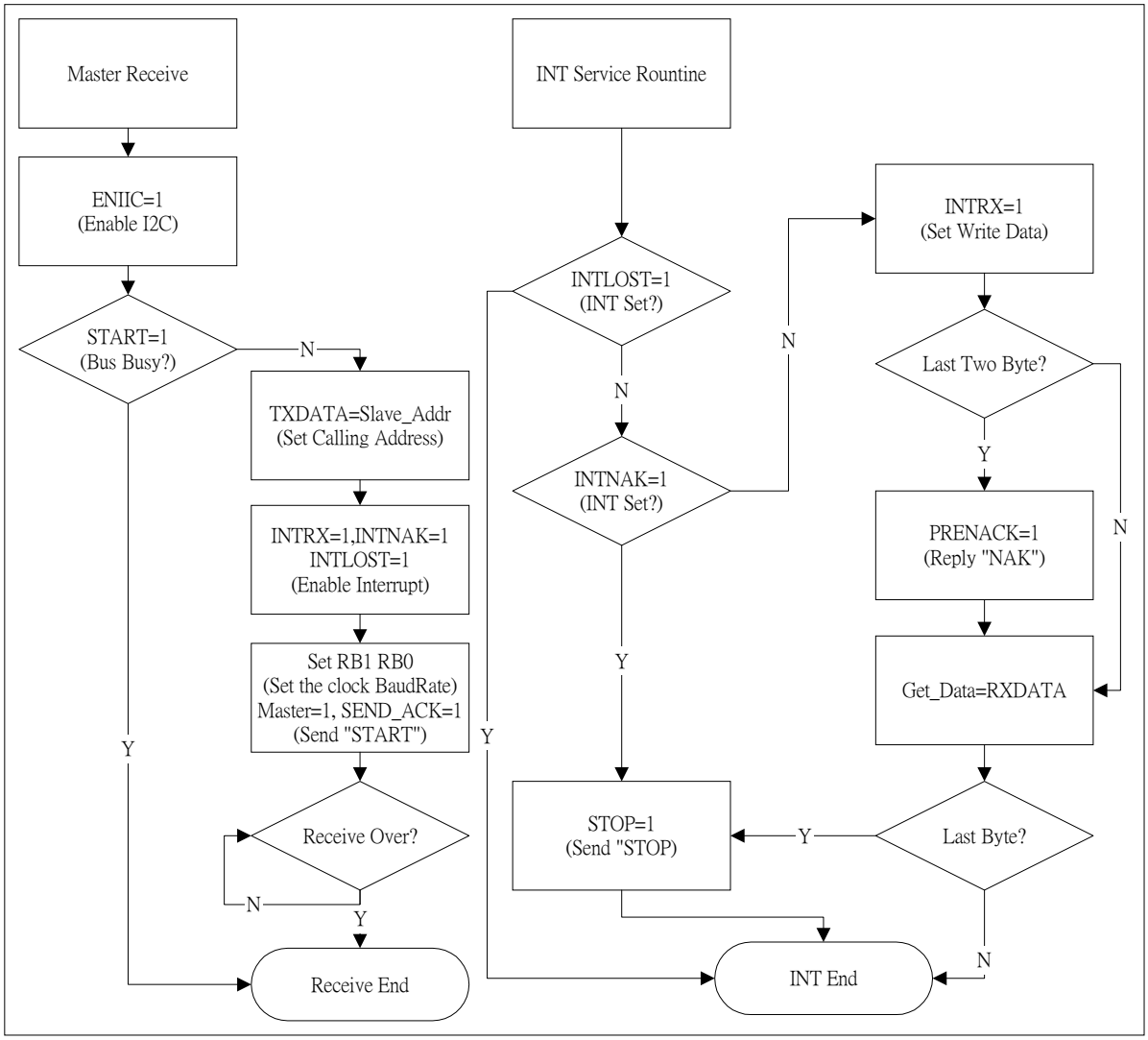
Flow Chart of I²C Master-Transmitter



Note:

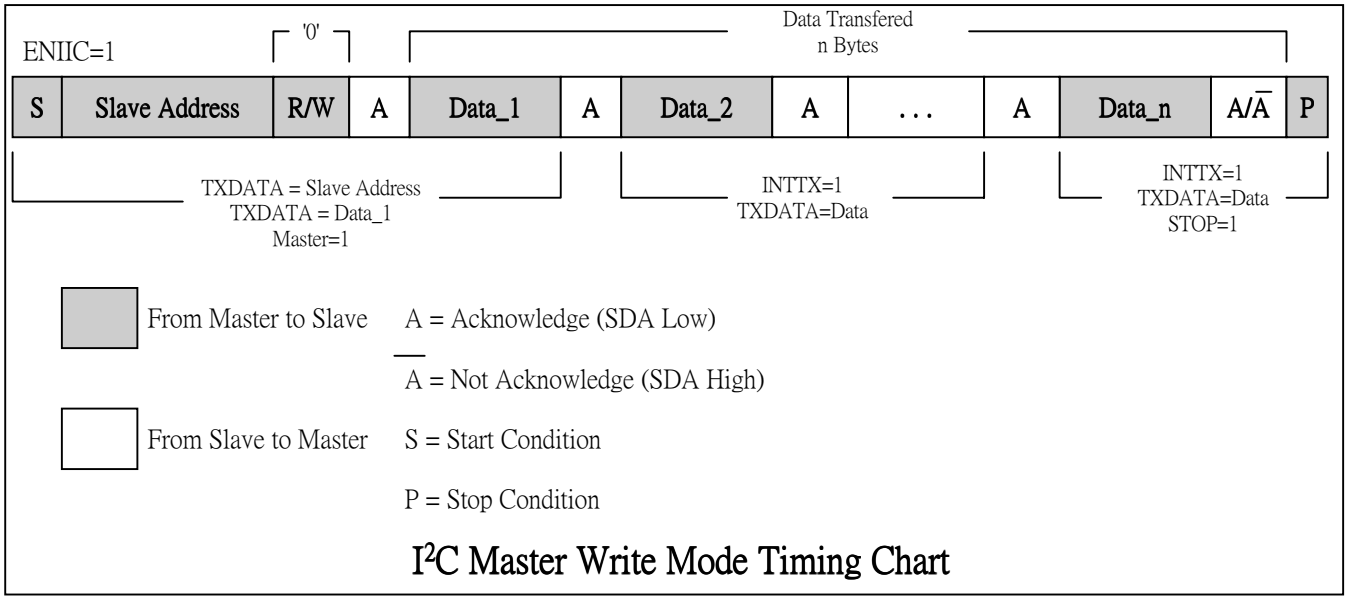
1. In our design, we reserve two level shift registers to make the transmission efficently. So you can try to write two byte data in the same time if the second level transmission buffer is empty (***TX_NULL=1***).
2. You can set the transmission clock baud rate and send “START” simultaneously.
3. The setting of the baudrate please refers to the following illustration about the control registers.
4. If you only want to transmit one data (Slave Address + Data), you can write the slave address and data first and then set the ***MASTER=1***, ***STOP=1*** simultaneously.
5. If you want to generate a “START” or “STOP” command on the bus line (No any data shift out), you can use the control register “***START_GEN***” and “***STOP_GEN***”.

Flow Chart of I²C Master-Receiver

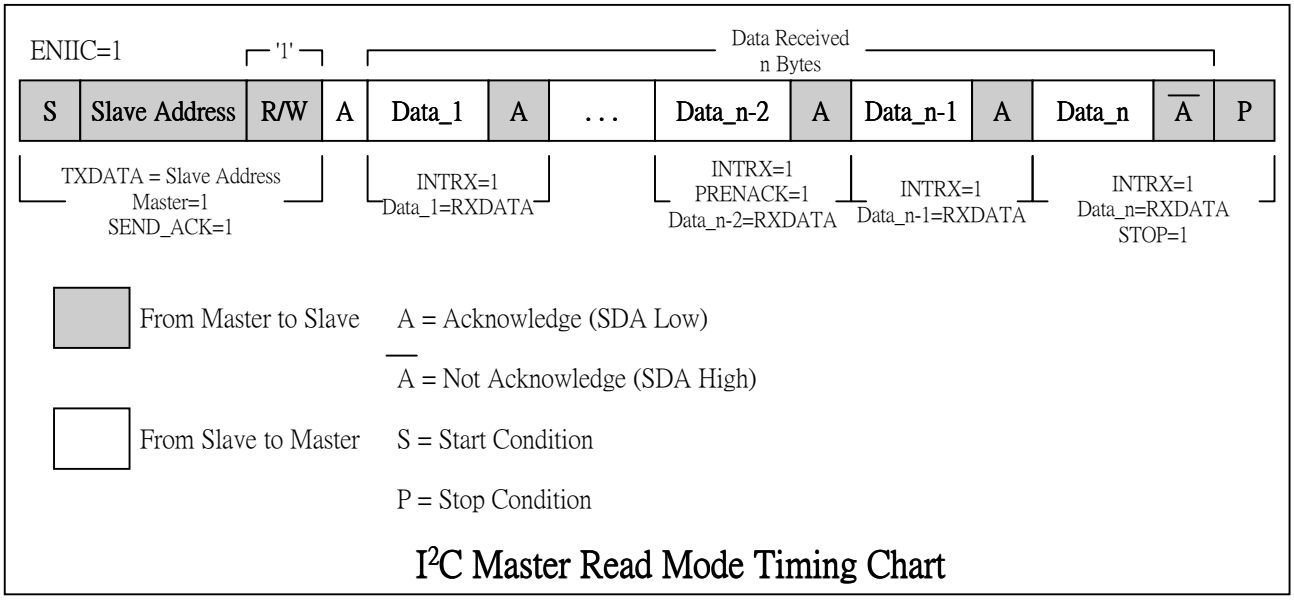


Note:

1. In our design, we reserve two level shift registers to make the reception efficently. So you can try to read two byte data in the same time if the second level reception buffer is full (***RX_NULL=1***).
2. You can set the transmission clock baud rate and send “START” simultaneously.
3. You need to reply a “NAK” command to the transmitter if you want to terminate the protocol. you need to set this bit ***PRENACK=1*** before you get the last two byte.
4. If you need to receive only one byte data, you don’t need to set ***SEND_ACK=1.***



I²C Master Write Mode Timing Chart



I²C Master Read Mode Timing Chart

Registers:

Register	IIC_CFG	I²C Bus Configuration Control Register	
B7	PRENACK	R/W	0: No effect 1: In master mode read mode, user need to set this bit in data sequency (n-2) (before you read out this data) to generate a “NACK” condition.
B6	SEND_ACK	R/W	0: Reply an “NACK” condition when the system acks as receiver 1: Reply an “ACK” signal when the system acks as receiver
B5	STOP	R/W	0: No effect 1: In master mode, I²C will generate a “STOP” signal.
B4	RESTART	R/W	0: No effect 1: Generating the “REPEAT START” signal
B3	RB1	R/W	Set the I²C bus transmission clock in master mode: RB1 RB0 BaudRate 1 1 400K 1 0 200K 0 1 100K 0 0 50K
B2	RB0	R/W	
B1	MASTER	R/W	0: No effect 1: Master mode. The I²C bus will switch to master mode and generate a “START” condition on bus line during the slave mode(ENIIC=1).
B0	WAIT	R/W	0: Release SDA line 1: Pull the SDA line low to generate a “WAIT” state manually.

Register	IIC_STATUS	I²C Bus Status Control Register	
B7	WRITE	R	0: Normal 1: The I²C is acked as a transmitter （sends data to the bus）
B6	READ	R	0: Normal 1: The I²C is acked as a receiver （receives data from the bus）
B5	TXDATA_NULL	R	0: Normal 1: The first level of the transmission buffer is empty (IIC_TXDATA)
B4	TX_NULL	R	0: Normal 1: The second level of the transmission buffer is empty
B3	RXDATA_FULL	R	0: Normal 1: The first level of the receive buffer is full (IIC_RXDATA)
B2	RX_FULL	R	0: Normal 1: The second level of the receive buffer is full
B1	BUS_START	R	0: Normal 1: There is a “START” condition on the I²C bus （A HIGH to LOW transmission on the SDA line while SCL is HIGH）
B0	BUS_STOP	R	0: Normal 1: There is a “STOP” condition on the I²C bus （A LOW to HIGH transmission on the SDA line while SCL is HIGH）

Register	INTIIC_EN	I²C Bus Interrupt Enable Control Register	
B7	INTA	R/W	0: Disable 1: Enable
B6	INTTX	R/W	0: Disable 1: Enable
B5	INTRX	R/W	0: Disable 1: Enable
B4	INTNAK	R/W	0: Disable 1: Enable
B3	INTLOST	R/W	0: Disable 1: Enable
B2	-	-	
B1	-	-	
B0	-	-	

Register	INTIIC_FLG	I²C Bus Interrupt Flag Control Register	
B7	INTA	R	0: No interrupt 1: When the calling address is same as the IIC_ADDR register
B6	INTTX	R	0: No interrupt 1: The transmission buffer is empty when the I²C is acked as transmitter
B5	INTRX	R	0: No interrupt 1: The receiving buffer is empty when the I²C is acked as receiver
B4	INTNAK	R	0: No interrupt 1: The system does not get a “ACK” signal when the I²C is acked as transmitter
B3	INTLOST	R	0: No interrupt 1: The system loses the arbitration when it acked as a master device. Note: If the master loses the arbitration, it will stop to generate the clock pulse.
B2	-	-	
B1	START_GEN	W	0: No effect 1: Force to generate a “START” signal on I²C bus and without send data out
B0	STOP_GEN	W	0: No effect 1: Force to generate a “STOP” signal on I²C bus

Register	INTIIC_CLR	I²C Bus Interrupt Flag Clear Control Register	
B7	INTA	W	0: No interrupt 1: Clear the “INTA” interrupt in INTIIC_FLG
B6	INTTX	W	0: No interrupt 1: Clear the “INTTX” interrupt in INTIIC_FLG
B5	INTRX	W	0: No interrupt 1: Clear the “INTRX” interrupt in INTIIC_FLG
B4	INTNAK	W	0: No interrupt 1: Clear the “INTNAK” interrupt in INTIIC_FLG
B3	INTLOST	W	0: No interrupt 1: Clear the “INTLOST” interrupt in INTIIC_FLG
B2	CLR_TX_FIFO	W	0: No effect 1: F/W straightly force to empty the transmission FIFO
B1	CLR_FIFO	W	0: No effect 1: F/W straigntly force to empty the TX/RX FIFO
B0	-	-	-

Register	IIC_TXDATA	I²C Bus Transmission Buffer Control Register	
B7	TXDATA7	W	I²C Bus Transmission buffer
B6	TXDATA6	W	
B5	TXDATA5	W	
B4	TXDATA4	W	
B3	TXDATA3	W	
B2	TXDATA2	W	
B1	TXDATA1	W	
B0	TXDATA0	W	

Register	IIC_RXDATA	I²C Bus Receiving Buffer Control Register	
B7	RXDATA7	R	I²C Bus Receiving buffer
B6	RXDATA6	R	
B5	RXDATA5	R	
B4	RXDATA4	R	
B3	RXDATA3	R	
B2	RXDATA2	R	
B1	RXDATA1	R	
B0	RXDATA0	R	

Register	IIC_ADDR	I²C Bus Slave Address Setting Control Register	
B7	ADDR7	R/W	Setting the 7 bits I²C slave address.
B6	ADDR 6	R/W	
B5	ADDR 5	R/W	
B4	ADDR 4	R/W	
B3	ADDR 3	R/W	
B2	ADDR 2	R/W	
B1	ADDR 1	R/W	
B0	ENIIC	R/W	0: Disble the I²C bus 1: Enable the I²C bus Note: You can reset the I²C machanism by clearing the ENIIC=0 then enable this bit ENIIC=1.

Section-12 DDC Port

12-1 General Description

This block is a 128/256-byte selectable dual-mode DDC Port. It is designed for use in applications requiring serial transmission of configuration and control information. Two modes of operation have been implemented:

- **Transmit Only Mode for DDC1,**
- **Bi-directional Mode for DDC2B,**

Upon power-up, the MCU needs to move the EDID data into the DDC RAM-Buffer from user's assigned EDID data ROM area and properly sets the DDC_CTRL and DDC_ADDR registers. The DDC-Port will be in the Transmit Only Mode, sending a serial bit stream of the entire RAM-Buffer contents, clocked by the VCLK signal. A valid high to low transition on the SCL pin will cause the device to enter the bi-directional Mode, with byte selectable read/write capability of the memory in standard I^2C bus protocol. It also enables the user to write-protect the entire RAM-Buffer contents by using the write-protect bit **WPT_DDC=1**.

12-2 Functional Description

The DDC Port operates in two modes, the Transmit-Only Mode and the bi-directional Mode. After users set the **EN_DDC=1** then the DDC function will be enabled.

There is a separate two-wire protocol to support each mode, each mode has a separate clock input but shares a common data line (SDA). The device enters the Transmit-Only Mode upon power-up. In this mode, the device transmits data bits on the SDA pin in response to a clock signal on the VCLK signal.

The device will remain in this mode until a valid high to low transition is placed on the SCL input. When a valid transition on SCL is recognized, the device will switch into the bi-directional Mode. If necessary, the user can switch the DDC port back to the Transmit-Only Mode (DDC1) by setting the **MODE_DDC=0** in DDC_CON register. Users can also set the **EN_BACK=1** in DDC_CON register, if an invalid DDC2 transmission occurs in the DDC port, the system will automatically go back to DDC1 after 128 VCLK signal.

Users can enable the DDC Port in bi-directional mode (DDC2) directly by setting the control register **MODE_DDC=1**.

12-2.1 Transmit-Only MODE

The device will power up in the Transmit-Only Mode at address 00H. This mode supports a unidirectional two-wire protocol for continuous transmission of the contents of the memory array. This device requires it be initialized prior to the valid data being sent in the Transmit-Only Mode. In this mode, the data is transmitted on the SDA pin in 8-bit bytes, with each byte followed by a ninth, null bit. The clock source for the Transmit-Only Mode is provided on the VCLK signal, and a data bit is outputted on the rising edge of VCLK. The eight bits in each byte are transmitted most significant bit first. Each byte within the RAM-Buffer will be outputted in sequence. When the last byte in the RAM-Buffer is transmitted, the internal address pointers will wrap around to the first RAM-Buffer location (00H) and continue the operation.

- **LEN_EDID = 0** ➨ 128-Byte Buffer Size (00H ~ 7FH)
- **LEN_DDiD = 1** ➨ 256-Byte Buffer Size (00H ~ FFH)

12-2.2 Bi-Directional Mode

The DDC Port can be switched into the bi-directional Mode by applying a valid high to low transition on the bi-directional Mode Clock (SCL) or set the control register **MODE_DDC=1**. When the device is in the bi-directional Mode, the VCLK input is disregarded. This mode supports a two-wire bi-directional data transmission protocol (I^2C-bus). In this protocol, a device that sends data on the bus is defined to be the transmitter and a device that receives data from the bus is defined to be the receiver. The bus must be controlled by a master device, that generates the bi-directional Mode Clock (SCL), controls access to the bus and generates the START and STOP conditions, while the DDC Port acts as the slave. Both master and slave can operate as transmitter or receiver, but the master device determines which mode is activated. In this mode, the DDC Port only responds to commands for device **%1010 $b_3b_2b_1$X**.

☆ "**$b_3b_2b_1$**" is defined respectively "**ADDR_B3,ADDR_B2 and ADDR_B1**" in DDC_ADDR register.

☆ "X" is a Read/Write (X=1 / X=0) bit defined by I^2C-bus standard.

12-3 Bus Status Definition

The following bus protocol has been defined:

☆ Data transfer may be initiated only when the bus is not busy.

☆ During data transfer, the data line must remain stable whenever the clock line is HIGH. Changes in the data line while the clock line is HIGH will be interpreted as a START or STOP condition.

Accordingly, the following bus conditions have been defined.

☆ BUS NOT BUSY （A）

Both data and clock lines remain HIGH.

☆ START DATA TRANSFER （B）

A HIGH to LOW transition of the SDA line while the clock (SCL) is HIGH determines a START condition. All commands must be preceded by a START condition.

☆ STOP DATA TRANSFER （C）

A LOW to HIGH transition of the SDA line while the clock (SCL) is HIGH determines a STOP condition. All operations must be ended with a STOP condition.

☆ Data Valid （D）

The state of the data line represents valid data after a START condition, and the data line is stable for the duration of the HIGH period of the clock signal. The data on the line must be changed during the LOW period of the clock signal. There is one clock pulse per bit of data. Each data transfer is initiated with a START condition and terminated with a STOP condition.

☆ Acknowledge

Each receiving device, when addressed, is obliged to generate an acknowledge after the reception of each byte. The master device must generate an extra clock pulse which is associated with this acknowledge bit. The DDC Port has to pull down the SDA line during the acknowledge clock pulse in such a way that the SDA line is stable LOW during the HIGH period of the acknowledge related clock pulse. Of course, setup and hold times must be taken into account. A master must signal an end of data to the slave by not generating an acknowledge bit on the last byte that has been clocked out of the slave. In this case, the slave must leave the data line HIGH to enable the master to generate the STOP condition.

☆ Slave Address

After generating a START condition, the bus master transmits the slave address consisting of a 7-bit device code (%1010,$b_3b_2b_1$, see the DDC_ADDR Register) for the DDC-Port. The eighth bit of slave address determines whether the master device wants to read or write to the RAM-Buffer. The DDC Port monitors the bus for its corresponding slave address continuously. It generates an acknowledge signal if the slave address was true and it is not busy.

12-4 Error Recovery Mode

The DDC Port will have a DDC2 transition state on entry DDC2 locked mode from which it can revert to DDC1 mode if it receives **128 VCLK pulses**, while the SCL line is idle. If the monitor sees a valid DDC2 control byte, it will lock into the DDC2 and thereafter disregard VCLK. When the system in the DDC2 transition state, the count of VCLK pulses shall be reset by any activity on the SCL line. The purpose of this option is to allow recovery of a system with a DDC1 host in which a spurious noise causes the display to enter the DDC2 mode.

- The DDC Port H/W will automatically switch back to the DDC1 mode when the **EN_BACK=1** is set.
- User also can disable the auto function by clearing **EN_BACK=0**, manually clear **MODE_DDC=0** to switch back to the DDC1 mode from the DDC2 mode.

12-5 Write Operation

12-5.1 Byte Write

Following the start signal from the master, the slave address and the R/W bit which is a logic low are placed onto the bus by the master transmitter. This indicates to the addressed slave receiver that a byte with a word address will follow after it has generated an acknowledge bit during the ninth clock cycle. Therefore, the next byte transmitted by the master is the word address and will be written into the **address pointer** of the DDC-Port. After receiving another acknowledge signal from the DDC-Port, the master device will transmit the data word to be written into the addressed RAM-Buffer location. The DDC-Port acknowledges again after completing write cycle and the master generates a stop condition.

12-5.2 Page Write (Sequential Write)

The write control byte, word address and the first data byte are transmitted to the DDC-Port in the same way as in a byte write. But instead of generating a stop condition the master transmits up to eight data bytes to the DDC-Port. After the receipt of each word, the address pointer bits are internally incremented by one. If the master should transmit more than buffer size (128 words if LEN_DDC=0 / 256 words if LEN_DDC=1) prior to generating the stop condition, the address counter will roll over and the previously received data will be overwritten.

Note:

☆ If a page write command attempts to write across a physical page boundary(128/256 words depended on bit **LEN_EDID=0/1**) , the result is that the data wraps around to the beginning of the page (overwriting data previously stored there). It is therefore necessary for the application software to prevent page write operations that would attempt to cross a page boundary

☆ The DDC-Port is under Write-Protect Mode when **WPT_DDC=1**. The DDC-Port may generate an acknowledge after writing command but the written data will not be written into the DDC RAM-Buffer. The written data are written into the DDC RAM-Buffer and the bit **UPD_DDC=1** when **WPT_DDC=0**.

12-5.3 Acknowledge Polling

Since the device will not acknowledge during a write cycle, this can be used to determine when the cycle is complete (this feature can be used to maximize bus throughput). Once the stop condition for a write command has been issued from the master, the device initiates the internally timed write cycle. ACK polling can be initiated immediately. This involves the master sending a start condition followed by the control byte for a write command (R/W = 0). If the device is still busy with the write cycle, then no ACK will be returned. If the cycle is complete, then the device will return the ACK and the master can then proceed with the next read or write command.

12-6 Read Operation

Read operations are initiated in the same way as write operations with the exception that the R/W bit of the slave address is set to “1”. There are three basic types of read operations: current address read, random read and sequential read.

12-6.1 Current Address Read

The DDC Port contains an address counter/pointer that maintains the address of the last word accessed, internally incremented by one. Therefore, if the previous access (either a read or write operation) was to address n, the next current address read operation would access data from address n + 1. Upon receipt of the slave address with R/W bit set to one, the DDC Port issues an acknowledge and transmits the eight bit data word. The master will not acknowledge the transfer but does generate a stop condition and the DDC Port discontinues transmission.

12-6.2 Random Read

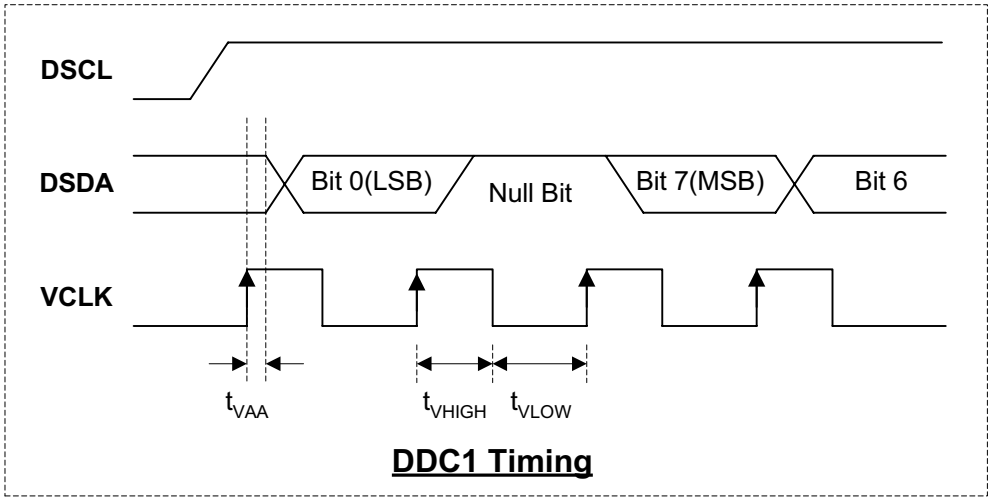
Random read operations allow the master to access any memory location in a random manner. To perform this type of read operation, the word address must be set first. This is done by sending the word address to the DDC Port as a part of the write operation. After the word address is sent, the master generates a start condition following the acknowledge. This terminates the write operation, but not before the internal address pointer is set. Then the master issues the control byte again with the R/W bit set to a one. The DDC Port will then issue an acknowledge and transmit the eight bit data word. The master will not acknowledge the transfer but does generate a stop condition and the DDC Port discontinues transmission.

12-6.3 Sequential Read

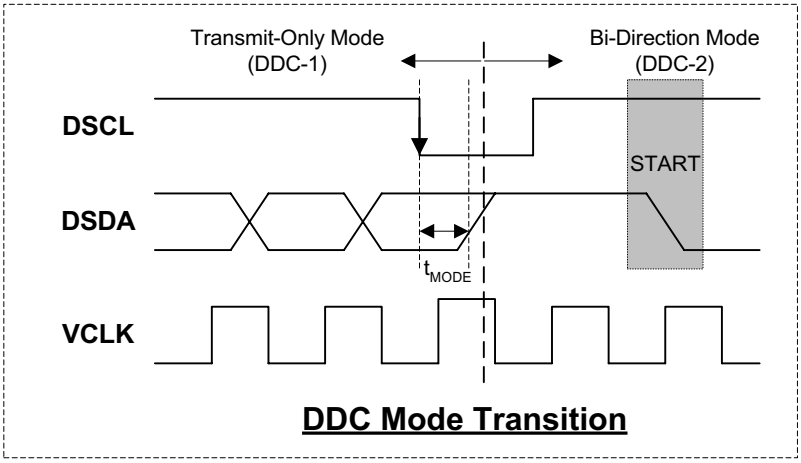
Sequential reads are initiated in the same way as a random read except that after the DDC Port transmits
the first data byte, the master issues an acknowledge as opposed to a stop condition in a random read. This directs the DDC Port to transmit the next sequentially addressed 8-bit word. To provide sequential reads, the DDC Port contains an internal address pointer which is incremented by one at the completion of each operation. This address pointer allows the entire RAM-Buffer contents to be serially read during one operation.

12-7 Noise Protection

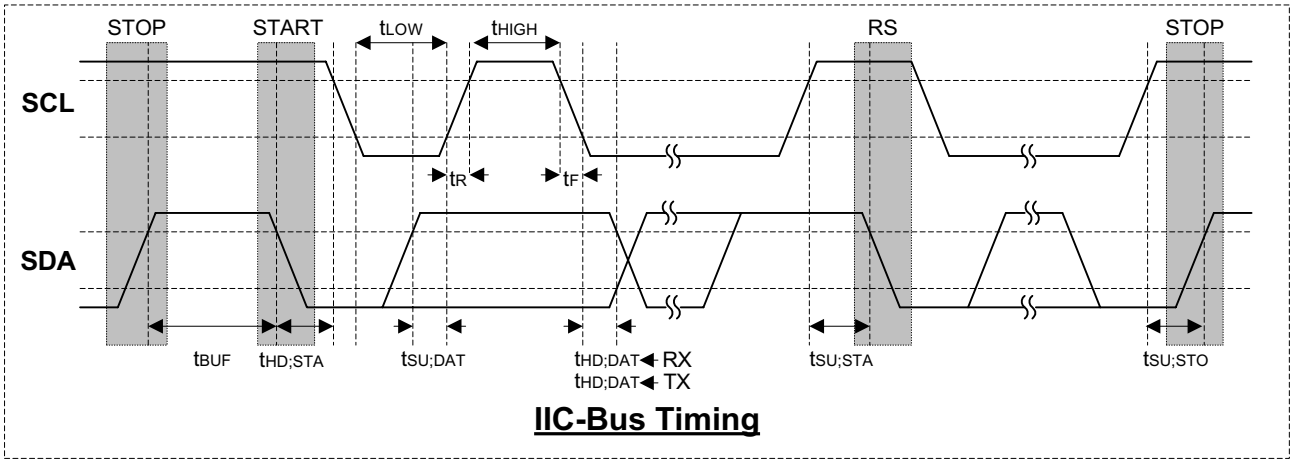
The SDA, SCL and VCLK inputs have Schmitt trigger and filter circuits, which can suppress the noise spikes to assure proper device operation even on a noisy bus.



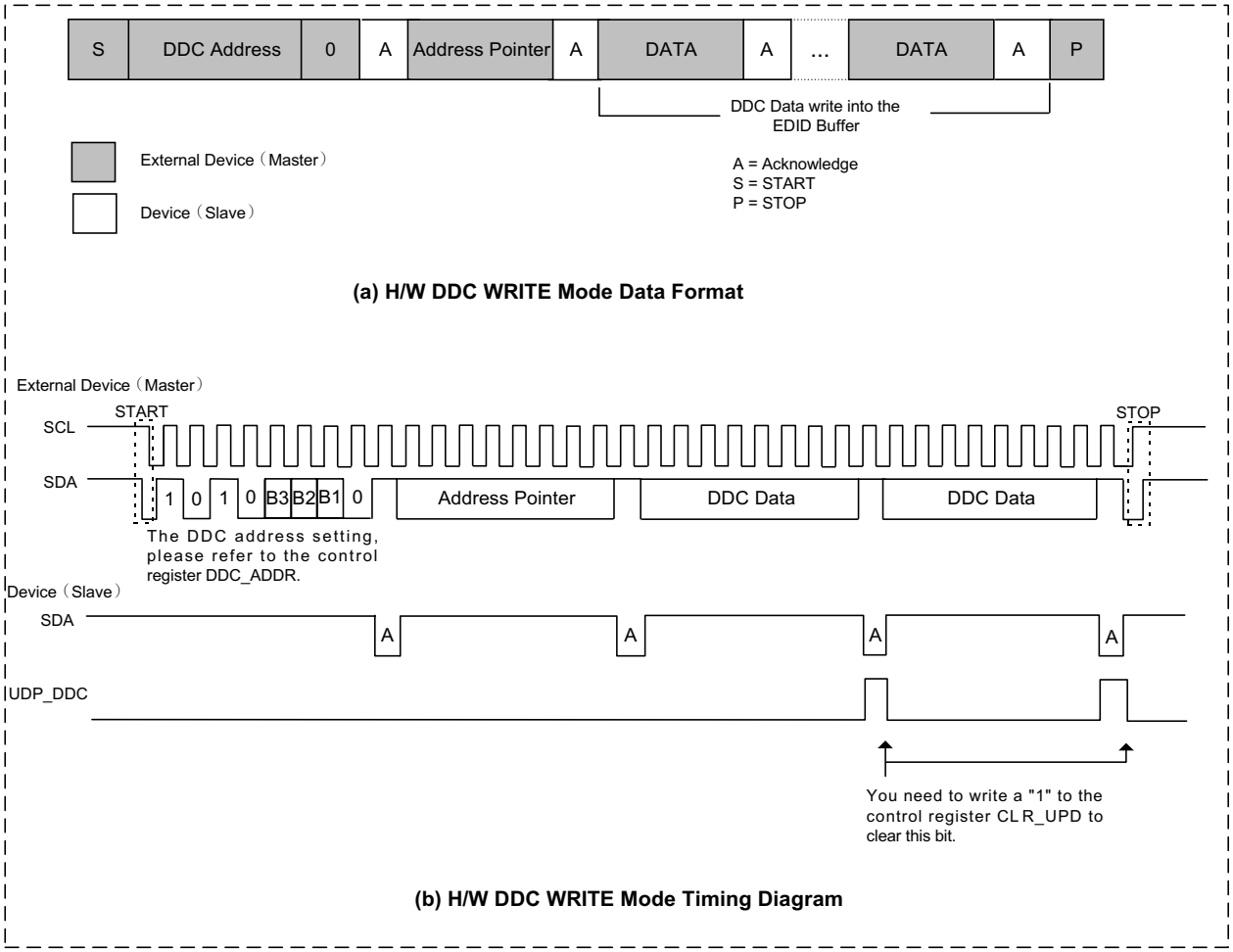
DDC1 Timing



DDC Mode Transition



IIC-Bus Timing



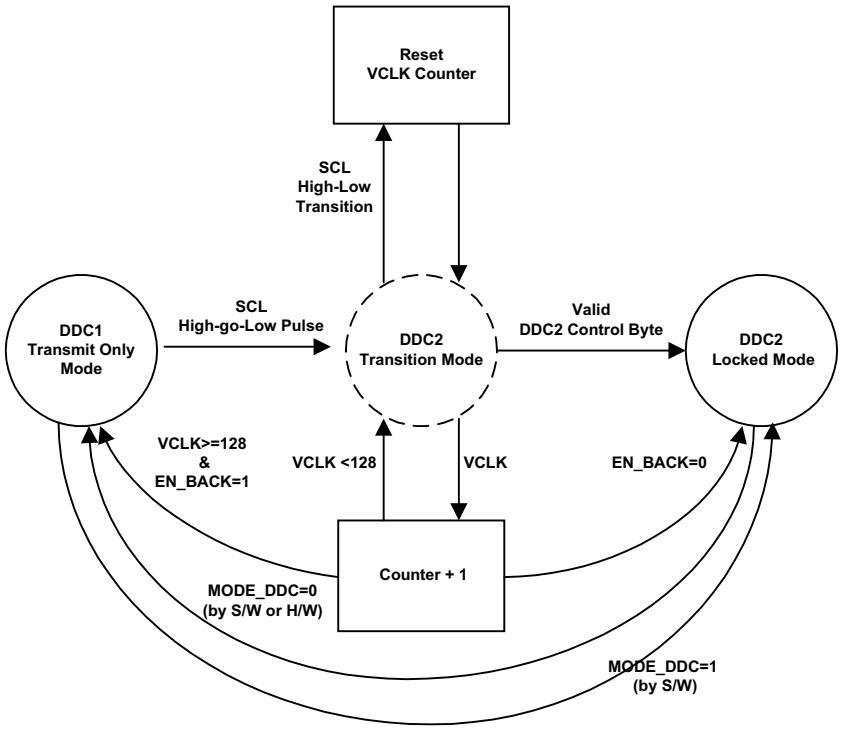
(a) H/W DDC WRITE Mode Data Format

(b) H/W DDC WRITE Mode Timing Diagram

Registers:

Register	DDC0/1_CTRL	DDC0/1 Control Register	
B7	EN_DDC	W/R	0:Disable DDC Port 1:Enable DDC Port ✍ During EN_DDC=0, the SDA and the SCL will be in a high impedance state.
B6	WPT_DDC	W/R	0:DDC RAM-Buffer is R/W Mode 1:DDC RAM-Buffer is read only under Write–Protect Mode (only for DDC)
B5	LEN_EDID	W/R	0:EDID Data length = 128 Bytes 1:EDID Data length = 256 Bytes
B4	MODE_DDC	W/R	DDC-Mode Control Bit 0:DDC1 H/W ➨ a default state after system reset S/W ➨ clear this bit by S/W to force into DDC1 mode 1:DDC2 H/W ➨ automatically set this bit when SCL go-low pulse is detected S/W ➨ set by SW to force into DDC2B mode
B3	EN_BACK	W/R	Enable Bit for automatically Switching Back to DDC1 Mode if VCLK>128 0:Disable 1:Enable
B2	INVT_VCLK	W/R	The VCLK Invert control bit for DDC1 communication 0: the polarity of the VCLK is the same as the one of the VSYNCI 1: the polarity of the VCLK is inverted with the one of the VSYNCI
B1	CLR_PTR	W	Clear the contents of the **Address Pointer** of the DDC RAM-Buffer 0:No effect 1:Clear it once after writing an 1 into this bit
B0	UPD_DDC	R	RAM-Buffer contents Updated Flag(set by H/W) 0:not Updated 1:Updated (only for DDC)
	CLR_UPD	W	Clear bit of the UPD_DDC bit 0:No Effect 1:Clear the UPD_DDC flag

Register	DDC0/1_ADDR	DDC0/1-Port Slave Address Register	
B7	VALID_B3	W	Valid/Mask Bit3,2,1 of slave address for DDC-Port Addressing 0:Masked: The respective address bits (ADDR_B3, 2 and 1 at register DDC_ADDR) will be Don't Care for DDC-Port addressing. 1:Valid: Otherwise, they will be valid address bits of the DDC-Port.
B6	VALID_B2	W	
B5	VALID_B1	W	
B4	X	-	Reserved
B3	ADDR_B3	W	Slave Address Bit-3~1 of the DDC Port These 3 lower order bits of the 7-bit slave address can be masked to compare with the written address from the master if the respective VALID bits within DDC_CON register are logic 0. ✧**The default value of the high order bit is %1010.**
B2	ADDR_B2	W	
B1	ADDR_B1	W	
B0	X	-	Unused



State Diagram of the H/W DDC Port

Section-13 Electrical Specifications

Absoulate Maximum Rating*

DC Supply Voltage ..... –0.3V to +5.5V

Input/Output Voltage ..... GND-0.2V to VCC+0.2V

Operating Ambient Temperature... 0°C to 70°C

Storage Temperature…….-55°C to 125°C

Operating Voltage ..... +3.0V to +3.6V

*Comments

Stresses above those listed under “Absoulate Maximum Rating” may cause permanent damage to the device. There are stress ratings only. Functional operation of this device at these or any other conditions above those indicated in the operational sections of this specification is not implied and exposure to absoulte maximum rating conditions for extended periods may affect device reliability.

13-1 DC Electrical Characteristics (VCC = 3.3V, T_A = 25°C, Oscillator freq. = 12MHz, Unless otherwise specified)

Symbol	Parameter	Min.	Typ.	Max.	Unit	Conditions
IDD	Operating Current	-	20	-	mA	No Loading
I/O Port						
Symbol	**Parameter**	**Min.**	**Typ.**	**Max.**	**Unit**	**Conditions**
$V_{UT(SYNC)}$	Schmitt Lower-Threshold Voltage for SYNC Inputs	1.5	-	1.9	V	HSYNCI,VSYNCI
$V_{LT(SYNC)}$	Schmitt Upper-Threshold Voltage for SYNC Inputs	0.8	-	1.2	V	HSYNCI,VSYNCI
$V_{UT(PORT)}$	Schmitt Upper-Threshold Voltage for I/O Ports	1.9	-	2.3	V	PA0~PA3;PA4*~ PA7*; PB0~PB3; PC0*,PC1*,PC2~PC7; PD0~PD6; PE0~PE1; P30,P31,P34,P35; RSTB
$V_{LT(PORT)}$	Schmitt Lower-Threshold Voltage for I/O Ports	1	-	1.5	V	PA0~PA3;PA4*~PA7*; PB0~PB3; PC0*,PC1*,PC2~PC7; PD0~PD6; PE0~PE1; P30,P31,P34,P35; RSTB
$V_{UT(IIC)}$	Schmitt Upper-Threshold Voltage for I^2C bus Ports	1.9	-	2.3	V	PB4*/SCL0*;PB5*/SDA0*; PB6*/SCL1*;PB7*/SDA1*
$V_{LT(IIC)}$	Schmitt Lower-Threshold Voltage I^2C bus Ports	1	-	1.5	V	PB4*/SCL0*;PB5*/SDA0*; PB6*/SCL1*;PB7*/SDA1*

I/O Port						
Symbol	**Parameter**	**Min.**	**Typ.**	**Max.**	**Unit**	**Conditions**
V_{OH}	Output High Voltage for I/O Ports	2.5	-	-	V	PA0~PA3 @ I_{OH} = -4mA PB0~PB3 @ I_{OH} = -4mA PC2~PC7 @ I_{OH} = -4mA PD0~PD6 @ I_{OH} = -4mA PE0~PE1 @ I_{OH} = -4mA P30,P31,P34,P35 @ I_{OH} = -100uA
	Output High Voltage for Open-Drain Ports/PWMs	-	-	5	V	External Voltage for Open Drain Structure PA4*/PWM12*,PA5*/PWM13*, PA6*/PWM14*,PA7*/PWM15* PB4*/SCL0*;PB5*/SDA0* PB6*/SCL1*,PB7*/SDA1* PC0*,PC1*
$V_{OL(PORT)}$	Output Low Voltage for I/O Ports	-	-	0.4	V	PA0~ PA3 @ I_{OL} = +8mA PA4*~PA7* @ I_{OL} = +8mA PE0~PE1 @ I_{OL} = +8mA PB0~PB3 @ I_{OL} = +4mA PC0*,PC1*; PC2~PC7 @ I_{OL} = +4mA PD0~PD6 @ I_{OL} = +4mA PE0~PE1 @ I_{OL} = +8mA P30,P31,P34,P35 @ I_{OL} = +4mA
$V_{OL(IIC)}$	Output Low Voltage for I^2C bus Ports	-	-	0.4	V	@ I_{OL}=+3mA PB4*/SCL0*,PB5*/SDA0*,
		-	-	0.6	V	@ I_{OL}=+6mA PB6*/SCL1*;PB7*/SDA1*
R_{PH1}	Pull up Resistor @ Vi=1.5V	20	40	60	KΩ	PA0~PA3 PB0~PB3 PC2~PC7 PD0~PD5
R_{PH2}	Pull low Resistor	30	60	90	KΩ	HSYNCI,VSYNCI @ V_{IH}=1.5V
Reset						
Symbol	**Parameter**	**Min.**	**Typ.**	**Max.**	**Unit**	**Conditions**
V_{LVR}	Low-Voltage Reset Voltage for Power	2.0	-	2.8	V	

13-2 AC Electrical Characteristics (VCC=3.3V, TA=25°C, Oscillator freq.=12MHz, unless otherwise specified)

A/D Converter						
Symbol	**Parameter**	**Min.**	**Typ.**	**Max.**	**Unit**	**Conditions**
t_{CNVT}	A/D Conversion Time	-	-	12	us	
V_{OFFSET}	A/D Converter Error	-	-	1	LSB	
V_{LINEAR}	A/D Input Dynamic Range of Linearity Conversion	GND	-	VCC	V	
Reset Block						
Symbol	**Parameter**	**Min.**	**Typ.**	**Max.**	**Unit**	**Conditions**
$t_{PW(RSTB)}$	Active-Low External Reset Pulse Width	-	64	-	t_{OSC}	
$t_{RST(POR)}$	Internal Reset Interval for Power-On Reset	-	2^{16}	-	t_{OSC}	
$t_{RST(WDT)}$	Watch-Dog Reset Period	500	520	540	ms	f_{OSC} = 12MHz
H/V Sync Processor						
Symbol	**Parameter**	**Min.**	**Typ.**	**Max.**	**Unit**	**Conditions**
$t_{DELAY(VSYNC)}$	Leading-edge delay between Vsync input and Vsync output	-	-	40	ns	This is a fixed delay
$t_{DELAY(HSYNC)}$	Leading-edge delay between Hsync input and Hsync output	-	-	40	ns	This is a fixed delay
$F_{VSYNC(SEP)}$	Vsync Frequency from Separate VSYNCI input for Sync Processor	15	-	250	Hz	Vsync Duty Cycle = 40%
f_{VCLK}	Vsync Input Frequency for DDC-1 Mode	-	-	25	KHz	Supply VCLK for DDC-1 mode only
$t_{VPW(SEP)}$	VSYNC input Pulse Width of Separate SYNC	0.150	-	32000	us	Vsync Duty Cycle < 40%
$t_{VPW(COMP)}$	VSYNC input pulse width of Composite SYNC	0.150	-	2000	us	Vsync Duty Cycle < 40%
f_{HSYNC}	Hsync Input Frequency	15	-	250	KHz	Hsync Duty Cycle = 40%
$t_{HPW(SEP)}$	HSYNC input Pulse Width of Separate-Type SYNC	0.150	-	85	us	Hsync Duty Cycle < 40%
$t_{HPW(COMP)}$	HSYNC input Pulse Width of Composite SYNC	0.150	-	20.8	us	Hsync Duty Cycle < 40%
$t_{HPW(COMP)}$	HSYNC input Pulse Width of Clamp Pulse Output	0.250	-	20.8	us	Hsync Duty Cycle < 40%
t_{PRE-EQ}	Period of Pre-Equalization Pulses	-	0.5	-	t_{HSYNC}	$t_{HSYNC} = 1 / f_{HSYNC}$

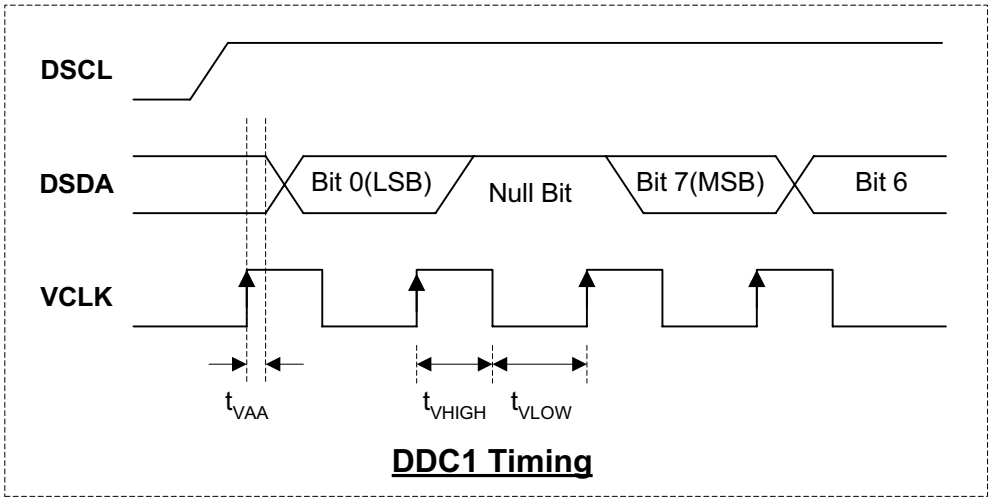
H/V Sync Processor						
Symbol	**Parameter**	**Min.**	**Typ.**	**Max.**	**Unit**	**Conditions**
$t_{POST-EQ}$	Period of Post-Equalization Pulses	-	0.5	-	t_{HSYNC}	$t_{HSYNC} = 1 / f_{HSYNC}$
$t_{INTVL(PRE-EQ)}$	Interval of Pre-Equalization Pulses	-	-	2	ms	
$t_{INTVL(POST-EQ)}$	Interval of Post-Equalization Pulses	-	-	2	ms	
$t_{PW(PRE-EQ)}$	Pre-Equalization Pulse Width	-	-	40%	t_{PRE-EQ}	$t_{PRE-EQ} = 0.5\ t_{HSYNC}$
$t_{PW(POST-EQ)}$	Post-Equalization Pulse Width	-	-	40%	$t_{POST-EQ}$	$t_{POST-EQ} = 0.5\ t_{HSYNC}$
t_{SERR}	Period of Single Serration Pulse	-	1	-	t_{HSYNC}	$t_{HSYNC} = 1 / f_{HSYNC}$
t_{SERR}	Period of Double Serration Pulse	-	0.5	-	t_{HSYNC}	$t_{HSYNC} = 1 / f_{HSYNC}$
$t_{PW(SERR)}$	Duty Cycle of Serration Pulse	-	-	40%	t_{SERR}	Either Single or Double Serration
$t_{VP\_DET(COMP)}$	Detect Time of Composite V-Polarity	-	-	3	ms	After a stable Hsync interval

DDC1 Mode:

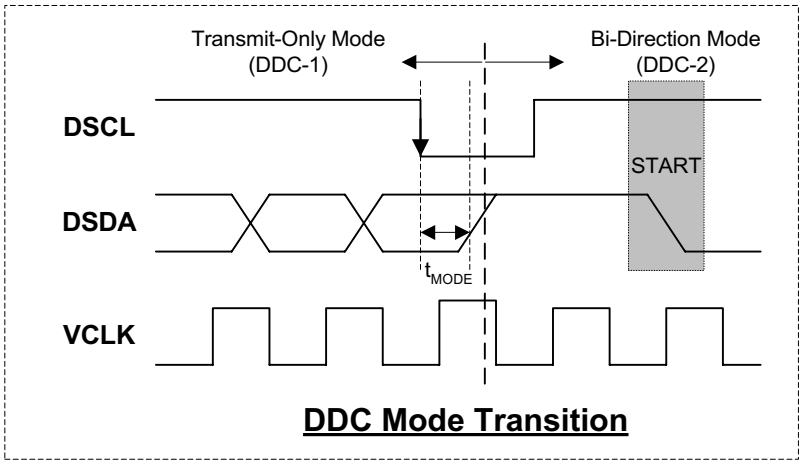
Symbol	Parameter	Min.	Typ.	Max.	Unit	Conditions
t_{VAA}	Data Valid from the low-to-high edge of the VCLK	-	-	1000	ns	
t_{MODE}	Time for Transition to DDC2B Mode from DDC1	-	-	500	ns	

Note:

VCLK comes from Separate VSYNCI or is extracted from Composite Sync. The internal noise filter will cause a filter time delay of the VCLK.



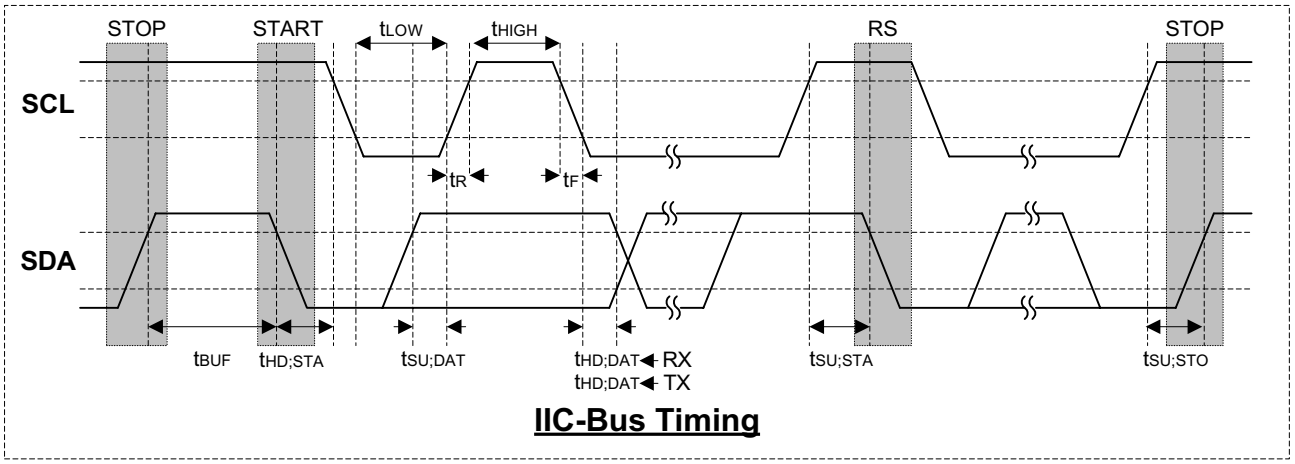
DDC1 Timing



DDC Mode Transition

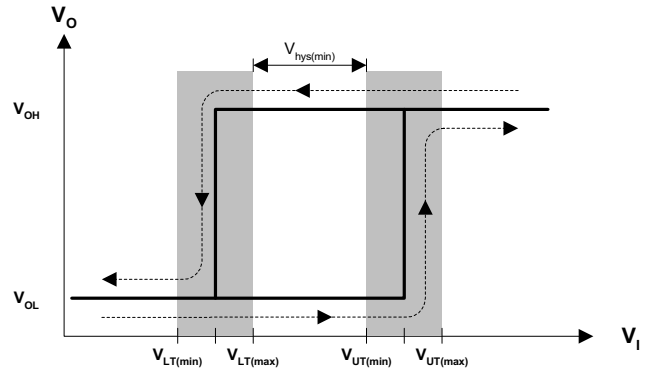
DDC2B+ Mode

Symbol	Parameter		Standard Mode		Fast Mode		Unit
			Min.	Max	Min	Max	
f_{SCL}	SCL Clock Frequency			100		400	KHz
t_{BUF}	Bus Free Between a STOP and START Condition		4.7		1.3		us
$t_{HD;STA}$	Hold Time for START Condition		4.0		0.6		us
t_{LOW}	LOW Period of The SCL Clock		4.7		1.3		us
t_{HIGH}	HIGH Period of The SCL Clock		4.0		0.6		us
$t_{SU;STA}$	Set-up Time for a Repeated START Condition		4.7		0.6		us
$t_{HD;DAT}$	Data Hold Time	Transmitter	0.1		0.1	0.9	us
		Receiver	0		0		
$t_{SU;DAT}$	Data Set-up Time		250		100		ns
t_r	Rise Time of Both SDA and SCL Signals			1000		300	ns
t_f	Fall Time of Both SDA and SCL Signals			300		300	ns
$t_{SU;STO}$	Set-up Time for STOP Condition		4.0		0.6		us
t_{SP}	Pulse Width of spikes which must be suppressed by the input filter		0	50	0	50	ns
C_I	Capacitance for each Bus Pin		-	10		10	pF
C_b	Capacitive load for each Bus Line		-	400		400	pF



IIC-Bus Timing

Symbol	Parameter	Standard Mode		Fast Mode		Unit
		Min.	Max	Min	Max	
$V_{IL(I2C)}$	Low Level Input Voltage	-0.5	1	-0.5	1	V
$V_{IH(I2C)}$	High Level Input Voltage	2.3	VCC+0.5	2.3	VCC+0.5	V
$V_{LT(I2C)}$	Schmitt Lower-Threshold Voltage for I^2C bus	1	1.5	1	1.5	V
$V_{UT(I2C)}$	Schmitt Upper-Threshold Voltage for I^2C bus	1.9	2.3	1.9	2.3	V
$V_{OL1(I2C)}$	Low Level Output Voltage @Io=3mA	0	0.4	0	0.4	V
$V_{OL2(I2C)}$	Low Level Output Voltage @Io=6mA	0	0.6	0	0.6	V
t_{OF}	Output Fall Time @Co=400pF		250		250	ns
I_I	Input Current @Vi=0.4 ~ 0.9VCC	-10	10	-10	10	uA



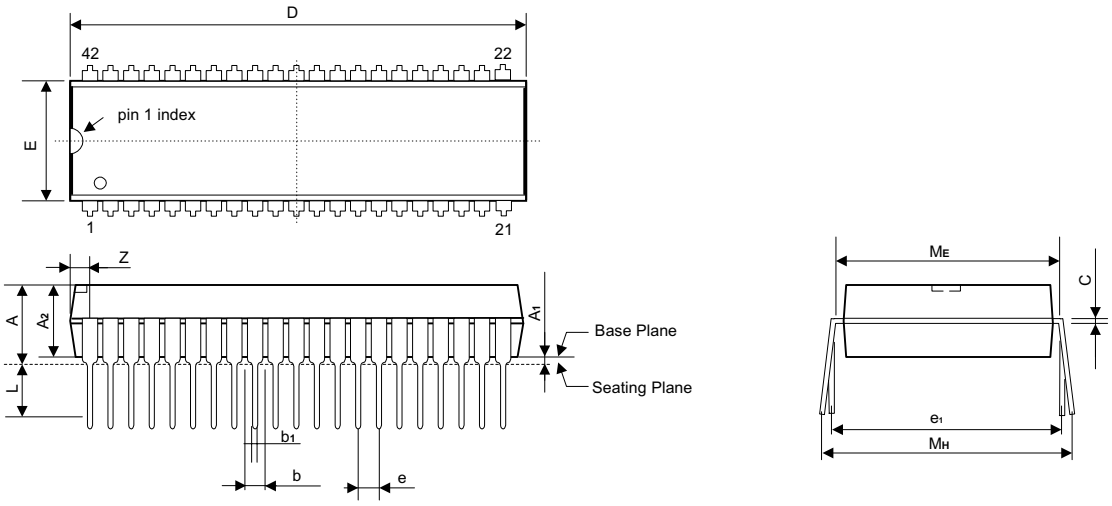
Schmitt Trigger Characteristics

Section-14 Ordering Information

Part No.	Package
NT68F632U	42L S-DIP
NT68F632L	44L PLCC

Section-15 Package Information

S-DIP 42L Outline Dimensions unit: inches/mm

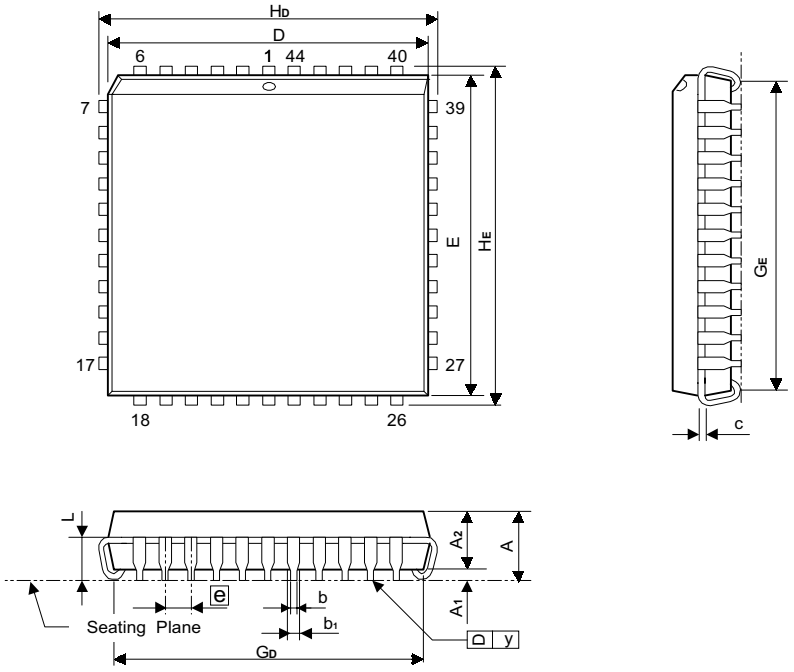


Symbol	Dimensions in inches	Dimensions in mm
A	0.200 Max.	5.08 Max.
A_1	0.020 Min.	0.51 Min.
A_2	0.157 Max.	4.0 Max.
B	0.051 Max.	1.3 Max.
	0.031 Min.	0.8 Min.
b_1	0.021 Max.	0.53 Max.
	0.016 Min.	0.40 Min.
C	0.013 Max.	0.32 Max.
	0.010 Min.	0.23 Min.
$D^{(1)}$	1.531 Max.	38.9 Max.
	1.512 Min.	38.4 Min.
$E^{(1)}$	0.551 Max.	14.0 Max.
	0.539 Min.	13.7 Min.
E	0.070	1.778
e_1	0.600	15.24
L	0.126 Max.	3.2 Max.
	0.114 Min.	2.9 Min.
M_E	0.622 Max.	15.80 Max.
	0.600 Min.	15.24 Min.
M_H	0.675 Max.	17.15 Max.
	0.626 Min.	15.90 Min.
W	0.007	0.18
$Z^{(1)}$	0.068 Max.	1.73 Max.

Notes : Plastic or metal protrusions of 0.25 mm maximum per side are not included.

PLCC 44L Outline Dimensions

unit: inches/mm



Symbol	Dimensions in inches	Dimensions in mm
A	0.185 Max.	4.70 Max.
A_1	0.020 Min.	0.51 Min.
A_2	0.150±0.005	3.81±0.13
b_1	0.028 +0.004 -0.002	0.71 +0.10 -0.05
b	0.018 +0.004 -0.002	0.46 +0.10 -0.05
c	0.010 +0.004 -0.002	0.25 +0.10 -0.05
D	0.653±0.010	16.59±0.25
E	0.653±0.010	16.59±0.25
e	0.050±0.006	1.27±0.15
G_D	0.610±0.020	15.49±0.51
G_E	0.610±0.020	15.49±0.51
H_D	0.690±0.010	17.53±0.25
H_E	0.690±0.010	17.53±0.25
L	0.100±0.010	2.54±0.25
y	0.006 Max.	0.15 Max.

Note:

1. Dimensions D and E do not include resin fins.
2. Dimensions G_D & G_E are for PC Board surface mount pad pitch design reference only.

Revision History

Version	Content	Date
1.0	First Formal Edition Release	July,2002
2.0	1. Cancel the LVR 12 clock detect, p.79. Detailed as follow.	October,2002

Version 2.0

Reset Block						
Symbol	**Parameter**	**Min.**	**Typ.**	**Max.**	**Unit**	**Conditions**
$t_{PW(RSTB)}$	Active-Low External Reset Pulse Width	-	64	-	t_{OSC}	
$t_{RST(POR)}$	Internal Reset Interval for Power-On Reset	-	2^{16}	-	t_{OSC}	
$t_{RST(WDT)}$	Watch-Dog Reset Period	500	520	540	ms	f_{OSC} = 12MHz

Version 1.0

Reset Block						
Symbol	**Parameter**	**Min.**	**Typ.**	**Max.**	**Unit**	**Conditions**
$t_{PW(RSTB)}$	Active-Low External Reset Pulse Width	-	64	-	t_{OSC}	
~~$t_{PW(LVR)}$~~	~~Drop-Down Pulse Width for LVR~~	~~-~~	~~12~~	~~-~~	~~t_{OSC}~~	~~Power < V_{LVR}~~
$t_{RST(POR)}$	Internal Reset Interval for Power-On Reset	-	2^{16}	-	t_{OSC}	
$t_{RST(WDT)}$	Watch-Dog Reset Period	500	520	540	ms	f_{OSC} = 12MHz